COTS® JOURNAL

Tech Focus: VME SBCs Roundup

Ethernet Melds LAND, SEA AND AIR NETWORKS

PLUS:

FPGAs Enable Configurable Designs

Gaming Graphics Fuel Military Simulation

Volume 8 Number 7 July 2006

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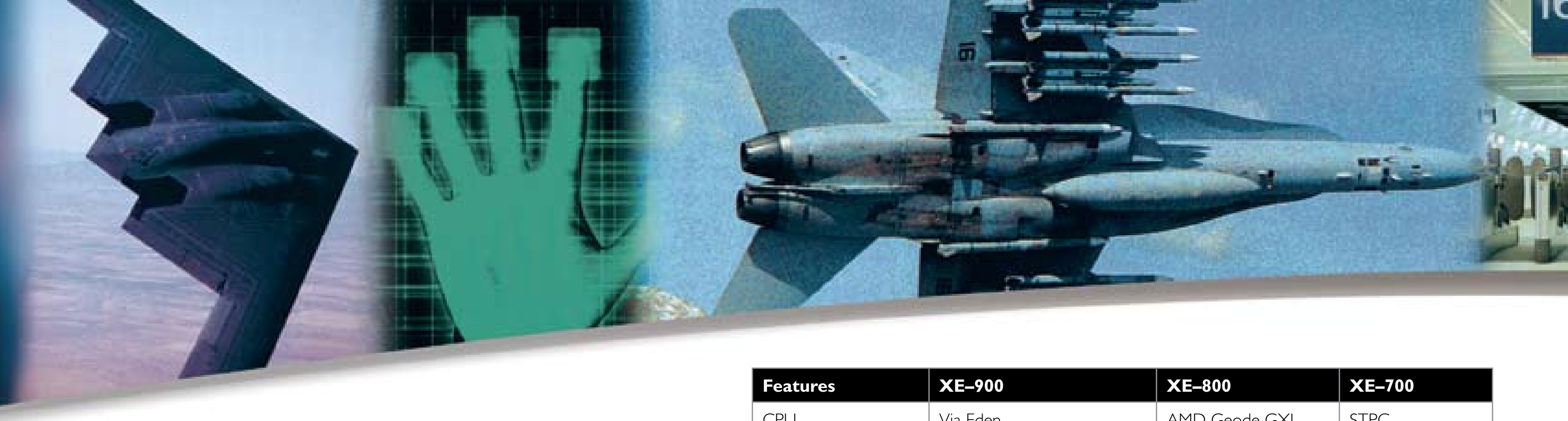

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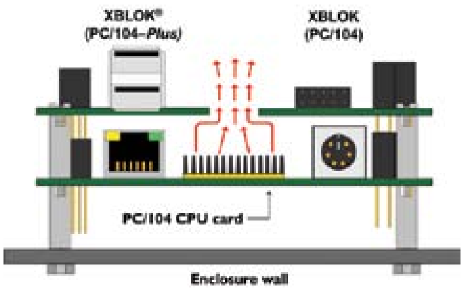

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COTS Journal

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COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

——**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

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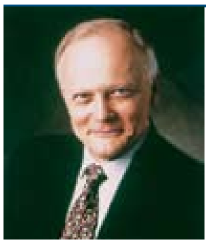
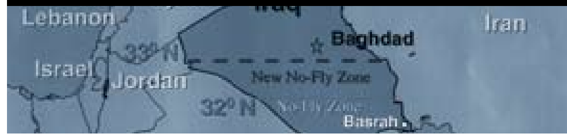
The 155mm Advanced Gun System (AGS) and the Long Range Land Attack Projectile (LRLAP), shown in this artist's rendering, together will enhance the Navy land attack capabilities for new DD(X) ships. The 155mm AGS with LRLAP will support U.S. Navy and Marine Corps expeditionary and joint operations warfighters in the littorals and deep inland. Precision fires and flexible response will also provide the support required for asymmetric operations.

(Photo courtesy of BAE Systems)





Publisher's

Notebook

Proud to Be an American

A few years ago when collecting data for our annual market survey, we talked to the people at Kennedy Space Center (KSC) about embedded computer products in the space industry. It's amazing how much embedded computing equipment is used in all sorts of support activities for the space industry. That trip opened up an opportunity to watch a Space Shuttle launch, which we deferred for a later time. Subsequent to that decision the Columbia tragedy occurred and that put going to KSC for a launch on indefinite hold.

Last month the opportunity for the *COTS Journal* editorial team to go to KSC for a shuttle launch re-emerged and we took it. I must confess that my attending had minimal benefit for *COTS Journal* or its readers, but it was great. Out of college I started out working for RCA Astro Electronics in New Jersey. There, I got to work on many civilian and military space/satellite projects. One of the more memorable ones was the Apollo Color Camera that ended up on the Lunar Rover. That program provided me with trips to the Cape, but unfortunately I never organized a trip for an Apollo launch. Chalk that up to youthful stupidity. Later I got to work on the Viking Mars Lander, which gave me a chance to converse with the late Dr. Carl Sagan. Those were significant events in my life and at the time I was sure that we would be walking on Mars before the century was out. Boy, was I wrong.

When it comes to memorable, meaningful work experiences, my trip earlier this month to see the launch of the Discovery on mission STS-121 fits right in there with working on Apollo and Viking. Our trip wasn't all play. We did get information on the next-generation vehicles that will replace the shuttle in 2010. There will be two basic launch vehicles: the Ares I, which will be the Crew Launch Vehicle and the Ares V, which will be the Heavy Lift Launch Vehicle—the "one (I)" and "five (V)" being an homage to the Saturn rockets of the Apollo program. NASA's budget has been very tight since the Apollo era. Right now it's around $4 billion, of which $1 billion were used for modifications to the shuttle since the Columbia accident.

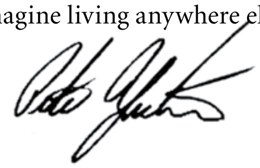
Tight funds means making everything you have last as long as it can and serve as many purposes as possible. But there should still be opportunities for our industry. Unlike military programs that somehow manage to suck up funds like there is no end, space programs—mostly support activities—are eager for the kind of cost-effective solutions that our industry has the opportunity to provide.

All that brings me to a complaint I must offer to my country's politicians. How can you sit in front of television cameras and bicker and complain about other politicians while "readjusting" the military budget to meet yours or your group's political ambitions at the expense of what the warfighters need to survive and to succeed? Just in case you don't get it, both political parties are guilty.

Get ready. Our industry is about to go back to an economic atmosphere like that of the early to mid-nineties. Back then many of the major suppliers to the military were starting to wonder what happened to all the money they used to get to supply products. There were unlimited ways to get more money out of the budget while supplying less. One key way was to buy less from the outside and produce more inside the organization. "The times they are a-changin'." As the funds faucet gets tighter, expect to hear the same whining and Chicken Little predictions that we heard last decade. Solutions that are more cost-effective—without sacrificing mission requirements—will start to take away contracts from suppliers who thought they had a lock on programs.

The entire military industry is being affected by the government's current undisclosed cash flow problem. And the government will continue playing a shell game with funds until the November elections are behind us (another complaint about politicians). Right now every politician is waiting for the other guy to flinch so they can make political hay, again at the expense of our warfighters. As soon as these elections are behind us, we're going to start playing catch-up on deliveries and improve program schedules that have been pushed out. Politicians will then start to get ready for the next election, and that will be the catalyst for tightening the funds spigot and ending some waste.

All that said, this is the greatest country on earth and our people are the most altruistic people on the planet. I'm proud to be an American, and watching the Shuttle take off on July 4th made me reflect and cement those feelings. As a nation we may not always do everything exactly like we think we should, but we're closer to doing what's right than anyone else. I couldn't imagine living anywhere else. ▮▮



Pete Yeatman, Publisher
COTS Journal

COTS JOURNAL

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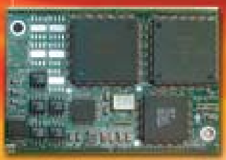
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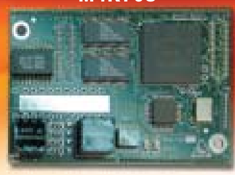

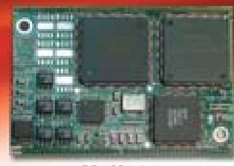
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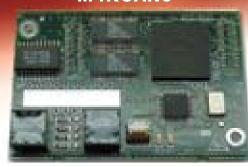

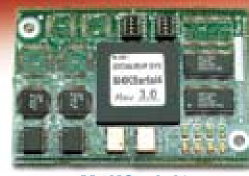
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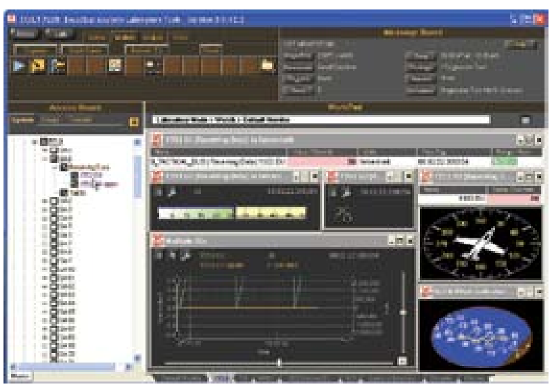
4000 Magic Plus Series

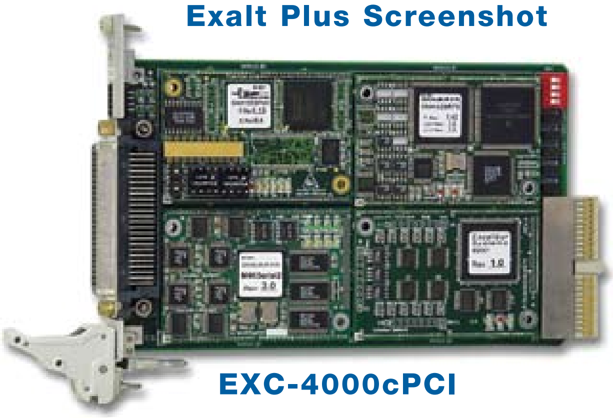
Last quarter there was a need for simulating seven MIL-STD-1553 Bus controllers on a VXI system. Next quarter they want to monitor 30 channels of Arinc-429 and two channels of Arinc-708 on a cPCI system. Next year you're looking at an integration project involving MIL-STD-1553, Discretes and Arinc-429 but the platform hasn't been selected yet. How do you handle the learning curves and risks associated with these different projects and still come up with with reasonable costs and manageable risk?

Excalibur's **EXC-4000** series was developed for just such needs. With baseboards available for PCI, cPCI, P104plus, VME and VXI moving from platform to platform is automatic. Software drivers hide all the internal system differences and present a common interface for all platforms.

Common modules snap into the baseboards to handle MIL-STD-1553/1760, Arinc-429, Arinc-708, CANbus, Discretes, H009, RS422/485/232 with more in development. Up to four modules fit onto a PCI/cPCI baseboard with up to eight modules on VME/VXI boards.


EXC-4000VME


Exalt Plus Screenshot


EXC-4000cPCI

Exalt Windows based software can handle all the above scenarios without any additional programming. It can monitor, record, compare and with **Exalt+** transmit to handle a variety of test and simulation needs. Multiple graphical formats for viewing the data ease analysis of the bus and built in tools help identify communications and data errors.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The Inside Track

Lockheed Martin Selects Symmetricom's Oscillator for MUOS Satellite Program

Symmetricom has announced that the company was chosen to supply its master reference oscillator for the Mobile User Objective System (MUOS) satellite led by Lockheed Martin for a U.S. Navy customer. MUOS is a next-generation narrowband tactical satellite communications system designed to significantly improve communications for U.S. forces on the move. Symmetricom's ultra-stable frequency reference was selected based on the program's cost, performance and schedule requirements.

The MUOS program significantly improves communications for warfighters while maintaining backward compatibility to the existing communications systems for the U.S. Department of Defense. MUOS will replace the current narrowband tactical satellite communications system known as the Ultra High Frequency Follow-On (UFO) system. Lockheed Martin Space Systems in Sunnyvale, CA., is the prime contractor and systems integrator for the MUOS program. The Navy's Program Executive Office for Space Systems, Chantilly, VA., and its Communications Satellite Program Office, San Diego, Calif., are responsible for the MUOS program. The first MUOS satellite is scheduled for on-orbit hand over to the Navy in 2010. Symmetricom is scheduled to deliver an engineering model of its master reference oscillator early this summer and qualification models in March 2007. Delivery of the first flight models is scheduled for August 2007.

Figure 1

Lockheed Martin is the prime for the U.S. Navy's Mobile User Objective System (MUOS), a next-generation narrowband tactical satellite communications system designed to significantly improve ground communications for U.S. forces on the move. MUOS satellites will provide the warfighter with the latest mobile technology such as simultaneous voice, video and data.

Symmetricom
San Jose, CA.
(408) 433-0910.
[www.symmetricom.com].

Thales and PrismTech Ink Middleware Development Deal

Thales and PrismTech have forged a strategic alliance that will see PrismTech independently develop and commercially exploit Thales's Data Distribution Service (DDS) middleware technologies. Thales in turn ensures the future competitiveness of their mission-critical systems through PrismTech packaging, enhancing and supporting them in an off-the-shelf product line. This new DDS product line is being launched by PrismTech and will be marketed under PrismTech's OpenSplice brand name.

For its part, Thales had been developing its own proprietary middleware solutions for mission-critical systems, but since the end of the 1990s, Thales has been following an open architecture strategy and has been heavily involved in the development of open standards. A significant part of this strategy was an active role in the standardization of the DDS specification at the Object Management Group (OMG) and the implementation of a DDS-compliant product, SPLICE-DDS, which leveraged more than fifteen years of publish-subscribe middleware deployment experience in Combat Management and Air Traffic Control Systems. Thales' business alliance with PrismTech is seen by both companies as a logical continuation of this strategy.

PrismTech
Burlington, MA.
(781) 270-1177.
[www.prismtech.com].

Thales
Toulon, France.
(33) 4 98 16 34 00.
[www.thalescomputers.com].

Boeing Selects Teledyne Controls for U.S. Navy P-8A AHMS Program

Boeing has selected Teledyne Controls for the development and supply of the Aircraft Health Monitoring System (AHMS) for the U.S. Navy P-8A Multi-Mission Maritime Aircraft (MMA). As the sole supplier, Teledyne will provide the hardware, software and engineering effort required to successfully support this multi-year program.

The AHMS solution offered by Teledyne Controls for the U.S. Navy MMA is an enhanced configuration of Teledyne's standard commercial Digital Flight Data Acquisition Unit (DFDAU), which is already flying on approximately half of the delivered Boeing 737NG aircraft serving the world airlines. Designed to collect and analyze flight data to monitor the condition of the

Figure 2

Based on the Boeing 737 BBJ, the P-8A Multi-Mission Maritime Aircraft (MMA) is a long-range anti-submarine warfare, anti-surface warfare, intelligence, surveillance and reconnaissance aircraft. It possesses an advanced mission system for maximum interoperability in battlespace.

aircraft, the DFDAU provides Boeing aircraft operators with a standardized hardware and software solution that allows for proactive maintenance and enhanced operation. Its ACMS Software, which offers extensive flexibility, enables users to specify the parameters they need for data monitoring, maintenance and operational efficiency, without the artificial constraints usually imposed by other software systems. The user-friendly operation and growth capacity of the Teledyne DFDAU will be instrumental in serving the P-8A mission requirements well.

Manufactured by Boeing and based on the Boeing 737 BBJ, the P-8A Multi-Mission Maritime Aircraft (MMA) is a long-range anti-submarine warfare, anti-surface warfare, intelligence, surveillance and reconnaissance aircraft. It possesses an advanced mission system for maximum interoperability in battlespace. Capable of broad-area, maritime and littoral operations, the P-8A MMA is expected to influence how the U.S. Navy's maritime patrol and reconnaissance forces train, operate and deploy.

Teledyne Controls
Los Angeles, CA.
(310) 820-4616.
[www.teledyne-controls.com].

Missile Defense Agency Awards Contract for Silicon-on-Diamond Work

Diamond Technologies, a supplier of wafer scale diamond and diamond products for solving thermal management challenges in high-performance applications, announces receipt of a $750,000 Phase II contract from the Missile Defense Agency (MDA) for GaN on silicon-on-diamond (SOD) development. The project will result in the delivery of GaN on SOD devices suitable for radar transmit/receive modules, as well as a documented process for producing GaN on SOD substrates and initial reliability data.

This award follows the company's work in Phase I of this important and timely MDA project, in which Sp3 delivered 100 mm SOD wafers with a GaN top surface. The company also delivered extensive modeling that demonstrated the significant performance advantages that are obtainable in a HEMT device built on a thermal layer of diamond. This modeling showed junction temperature drops of 80°K combined with a 37% increase in power.

Sp3 is supplying DOS wafers ranging in size from 50 mm to 300 mm for use in various research and development projects. These wafers are being used for developments in active device thermal management, MEMS structures and sensor applications. With a thermal conductivity that is 10X better than silicon and 2-3X better than Silicon Carbide, diamond films will provide a path for integrated thermal management in many applications that are becoming performance-limited by thermal issues.

Sp3 Diamond Technologies
Santa Clara, CA.
(408) 492-0630.
[www.Sp3inc.com].

Lockheed Martin Awards Data Recording Systems Contract to VMETRO

Lockheed Martin has awarded VMETRO a contract to supply Vortex Data Recording systems to support Lockheed Martin's work with the Aegis Ballistic Missile Defense (Aegis BMD) Weapon System. The Data Recording systems are based on VMETRO's Vortex VME Open Data Recording platform and include playback of the recorded data over 10 Gbit Ethernet. The Vortex system will be incorporated into Lockheed Martin's instrumentation and test plan for the Aegis BMD Signal Processor (BSP). The Aegis BSP is in development and will be installed in Aegis BMD ships beginning in 2010. It provides an advanced discrimination capability to defeat more complex ballistic missile threats. The Aegis BSP has performed flawlessly in ten "at-sea" test events over the last 12 months.

VMETRO's Applications Group will develop application-specific software for the record and playback requirements. This initial contract is valued at approximately $600,000 with additional systems expected over the course of the multi-year program. The Aegis Weapon System is the world's premier naval surface defense system and is the foundation for Aegis BMD, the primary component of the sea-based element of the United States' Ballistic Missile Defense System. The Aegis BMD Weapon System seamlessly integrates the SPY-1 radar, the MK 41 Vertical Launching System, the SM-3 missile and the weapon system's command and control system. When integrated with the U.S. Ballistic Missile Defense System, the Aegis BMD Weapon System receives cues from and provides cueing information to other BMDS elements. The Aegis Weapon System is currently deployed on 80 ships around the globe with more than 25 additional ships planned or under contract.

VMETRO
Houston, TX.
(281) 584-0728.
[www.vmetro.com].

Figure 3

A standard missile - 2 (SM-2) is launched from the Pearl Harbor-based Aegis cruiser USS Lake Erie (CG 70) as part of a U.S. Navy missile defense demonstration. The demonstration, in cooperation with the Missile Defense Agency, was the first sea-based intercept of a ballistic missile in its terminal phase.

COTS Websites

www.dtic.mil

DTIC Search Engine Is a "Google" for Military Technical Info

The Defense Technical Information Center (DTIC) was fielded with a daunting mission in mind: to sort and organize the DoD's array of technology-related activities, laboratories and information resources. Its Web site is the centerpiece of that mission. The DTIC provides centralized operation of DoD services for the acquisition, storage, retrieval and dissemination of Scientific and Technical Information (STI) to support DoD research, development, engineering and studies programs. And now it offers a feature called DTIC Search. It lets visitors search for science and technology information across all DoD sectors and beyond. This includes many defense agencies, unified commands, the military services—Army, Navy, Air Force, Marine Corps—and other elements of the defense and military establishments. It can also be configured to coordinate searches with your favorite search engine, such as Google or FirstGov, or even search only on ".mil" Web sites using those engines.

DTIC also hosts a variety of databases. Its Technical Report Database contains nearly two million reports in print and electronic form conveying the results of Defense-sponsored research, development, test and evaluation (RDT&E) efforts. DTIC has also acquired Library of Congress Federal Research Division records that cover a variety of foreign and domestic subject areas. A Research Summaries Database contains descriptions of DoD research that provide information on technical content, responsible individuals and organizations, principal investigators and funding sources at the work-unit level. And finally, DTIC's Independent Research and Development (IR&D) Database has over 165,000 descriptions of R&D projects initiated by DoD contractors but not performed under contract.

Defense Technical Information Center, Fort Belvoir, VA.
(800) 225-3842. [www.dtic.mil].

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Select photos courtesy of the U.S. Army and U.S. Navy.

Adapting Ethernet for the Battlespace

Commercially derived host offload and service performance protocols can be used to help adapt Gigabit Ethernet technology to the needs of military system design.

Steve Rood Goldman, Product Manager
High Speed Networking, Data Device Corp.

The growing interest in Ethernet for military applications has been driven by this networking technology's commercial success. Such ubiquity has resulted in readily available COTS software and hardware with attractive cost and performance characteristics.

However, commercial technology does not always meet military constraints, which has limited the military use of Ethernet to non-mission-critical applications. Fast Ethernet has already been deployed in several military systems, but designers want to take advantage of Gigabit Ethernet performance for critical functions such as sensor interfaces, display processing, digital map servers and data recorders. The transition to Gigabit Ethernet in the battlespace calls for designers to closely examine network performance requirements.

Quality of Service for the Battlespace

IP-based Ethernet networks provide best-effort service, which means that there are no inherent delay or throughput guarantees. But mission-critical functions, such as delivering data to a sensor processor and then over to a glass cockpit display, require tight bounds on data latency and jitter. Quality of service (QoS) refers to the performance of a network as perceived by the service user and is

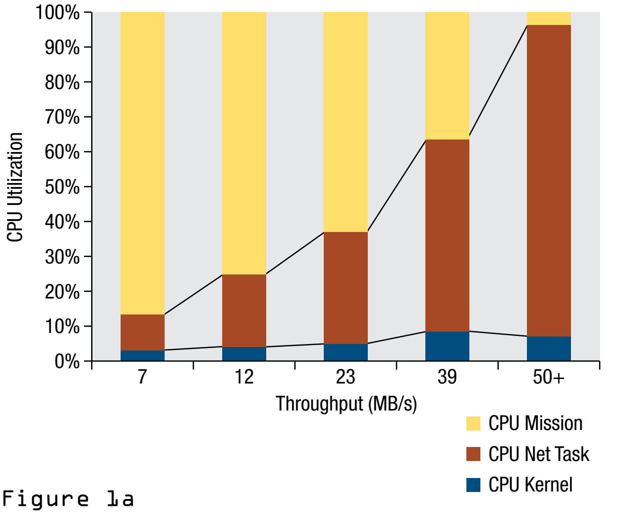

Figure 1a

CPU loading imposed by Ethernet protocol processing: native port performance.

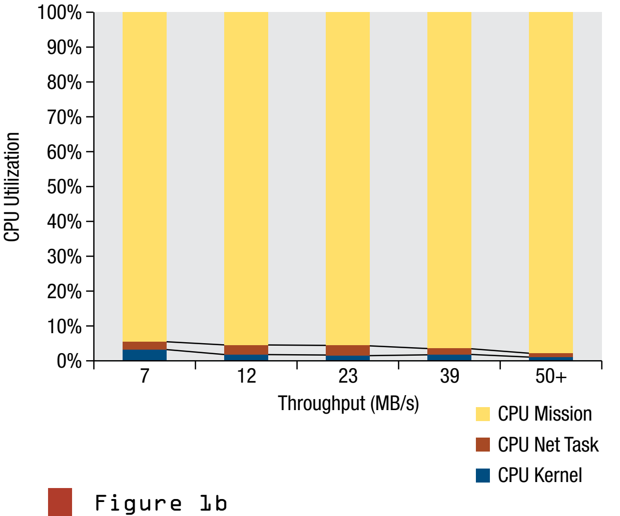

Figure 1b

CPU loading imposed by Ethernet protocol processing: offload port performance.

Figure 2

Data Device Corp.'s DDC ET-71000M2 Gigabit Ethernet TCP/IP Offload Engine PMC card.

determined by policies applied at various network elements.

One method of ensuring performance is to over-provision the network, increasing capacity well beyond average requirements. However, there are flaws with this approach. Line-rate throughput does not guarantee delay, such as the case where real-time video or sensor data is waiting for a low-priority transfer by a file server. The bursty nature of network traffic also means that at some point, congested links will occur no matter how overbuilt the network.

The use of Ethernet in commercial telecommunications and aircraft applications has lead to the development of QoS mechanisms that are adaptable to Ethernet in the battlespace. These mechanisms share a common theme: guaranteeing service quality requires that traffic be differentiated in some way. Protocols such as Integrated Services (IntServ) and ARINC-664 manage individual flows through the network. Flow management protocols manage the traffic streams for individual application connections. IntServ uses source and destination IP addresses while ARINC-664 defines a data link-layer Virtual Link (VL), which is a unidirectional connection between a single source and multiple destination nodes.

Both protocols offer guaranteed delay service, which requires that all of the network elements, end nodes, edge switches and core routers reserve resources for each flow. Maintaining fine-grained QoS seems well matched for military applications, but there are limitations. Managing numerous flows adds complexity to router designs and requires storing large volumes of network state information. For small, closed networks the level of complexity required to manage individual flows may be acceptable.

Differentiated Services (DiffServ) manages traffic at a higher level of granularity, using a small number of priority classes. Class-based traffic management provides coarse differentiation, which is handled at the edge of the network. Edge nodes classify packets, mark them with an appropriate priority and pass them to routers within the network core. The core routers forward traffic based on the marked priority instead of by individual flows. This approach reduces management complexity and is more easily scaled to large networks, but it allocates bandwidth statistically and cannot guarantee delay bounds.

Redundancy Mechanisms Improve Service Performance

Network availability also impacts service performance. A variety of redundancy mechanisms can be used to improve the availability of Ethernet IP networks. Most commonly, the Transaction Control Protocol (TCP) provides temporal redundancy by resending unacknowledged packets. Network routers use the Spanning Tree Protocol (STP) as a means of re-establishing connectivity after a network outage.

The STP protocol and its quicker replacement, Rapid Spanning Tree Protocol (RSTP), are not all that speedy, taking multiple seconds to converge. Critical applications cannot afford to lose seconds-worth of data waiting for routers to find a new path through the network after a link failure. The Link Aggregation Control Protocol (LACP), a method of logically bonding Ethernet links into a single high-bandwidth trunk, provides graceful degradation and failover capability. But again, the LACP messaging mechanism takes seconds to reconfigure the affected switches.

A more robust form of redundancy is implemented in the ARINC-664 networks used for critical functions on commercial aircraft. All traffic sent from a source node is duplicated and transmitted simultaneously over two paths. A sequence number is appended to the data packet, permitting receiving nodes to eliminate duplicates. Redundancy management is completely transparent to the application, which has no knowledge of packets being discarded. This form of redundancy is costly, since all network elements need to support double the number of links.

Loading Issues

Ethernet refers specifically to the physical and link layer operation of the network, but in practice, the definition has been extended to include the TCP/IP and UDP/IP protocols. These protocols enable inter-networking and provide flexibility, the root of Ethernet's popularity. These are complex protocols that manage fragmentation, reassembly, connection management, flow control and data retransmission.

Data link, or media access control (MAC), processing on a military SBC is managed by the system controller or the onboard Ethernet controller. The higher-level protocols, included as part of the system kernel, run on the processor along with the application program. At gigabit speeds, protocol processing can become a significant load on the processor, which can impair the performance of the mission function.

To demonstrate the severity of the CPU loading imposed by Ethernet protocol processing, measurements were made using two military SBCs configured with a 1 GHz 7455 CPU and a Marvell Discovery II system controller. Both SBCs were loaded with the VxWorks 5.5 RTOS. The native, built-in Gigabit Ethernet ports on the SBCs were connected through a managed switch for monitoring purposes. One SBC was used as the data transmitter and the other as the receiver. CPU loading was monitored as throughput was varied by adjusting message and data buffer sizes. In order to roughly simulate the behavior of an embedded system, a "mission function" was used to occupy as much of the CPU as possible by calculating the roots of polynomials.

The receive SBC results using the native Gigabit Ethernet port show that the impact of the Kernel task remains nearly flat as throughput is increased (Figure 1a). The NetTask, which includes the operation of the TCP/IP protocol stack, increases with throughput such that nearly the full capacity of the processor is used to receive data packets at speeds greater than 50 Mbytes/s. When a TCP/IP Offload Engine (TOE) device is used to replace the native port, less than 10% of the processor's capacity is used by the NetTask, leaving most of its capacity available for the CPU Mission function (Figure 1b).

TCP/IP Offload Engine Implementations

TOE implementations vary. Some use dedicated processing resources based on hard-wired implementations, such as commercial ASICs or FPGAs, and others use commercial processors. Tradeoffs to consider when comparing various implementation approaches include flexibility, application transparency, performance, life-cycle control and the ability to meet battlespace environmental requirements.

One example of a TOE is the DDC ET-71000 Gigabit Ethernet Network Access Controller (Figure 2). This mezzanine card, designed for rugged military applications, uses a processor-based TOE implementation to provide full, transparent offload of the protocol stack. Compared to commercial Ethernet controllers, the processor supports extended temperature operation and provides the flexibility needed to incorporate enhanced QoS and redundancy protocols.

Military system designers cannot achieve satisfactory results by simply dropping in commercial Gigabit Ethernet technology. Stringent performance bounds set military applications apart. Nevertheless, technology driven by commercial needs, including host offload and service performance protocols, are a good starting point for a solution and should be adapted to military use.

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Defense Platforms Get Ready for IPv4/v6

A shift from parallel buses to switched intra-platform network architectures is enabling the transformation to IPv6 in battlefield platforms. In VME systems, this has begun with the introduction of switched Gigabit Ethernet.

Nauman Arshad, Product Marketing Manager
Curtiss-Wright Controls Embedded Computing

Networks based on the Internet Protocol (IP) are already commonplace in both commercial and military enterprises where they help to enable seamless interoperability and communication among heterogeneous computers around the world. IP networks are rapidly finding their way into the core of many embedded defense platforms. No longer limited to the communications subsystem within the platform, IP promises to extend beyond it to unify box-to-box, blade-to-blade and CPU-to-CPU intra-platform networks.

The DoD's vision of network-centric warfare has shifted in emphasis beyond the effectiveness of an individual air, land or sea platform in the battlefield. That emphasis now includes the effectiveness of the "platform network" and how it connects into the "network-of-networks" that transcends all platforms and seamlessly ties them back into the DoD enterprise.

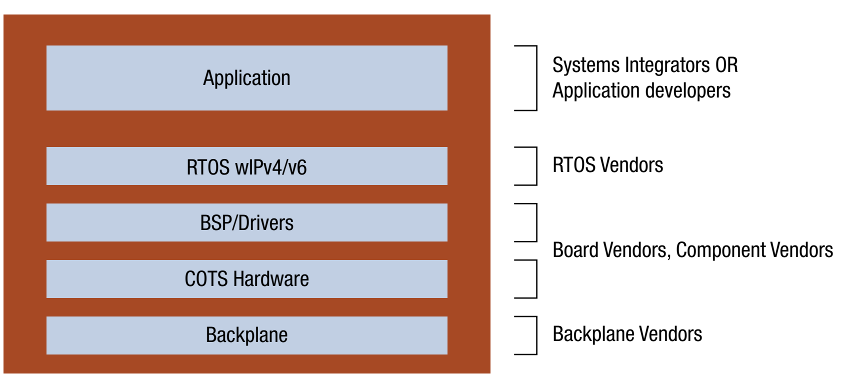

Figure 1

Key embedded building blocks in the multi-vendor ecosystem must become aligned for use in packet-switched, IPv4/v6-enabled network-centric applications.

Standards Shift From IPv4 to IPv6

The DoD's ultimate goal of network-centric warfare operations within the Global Information Grid (GIG) is to seamlessly connect its enterprise with heterogeneous platform resources in the battlefield by standardizing on IPv4 today and on IPv6 in the near future. This enhanced connectivity, combined with convergence on a unified protocol, will increase the lethality, situational awareness and knowledge superiority of defense forces.

The DoD has mandated the transition to IPv6 by purchasing networking equipment that is both IPv4- and IPv6-capable, with the goal of achieving full IPv6 compliance by 2008. The transformation of the DoD enterprise to IPv6 will clearly have its challenges and change will not happen overnight. However, the transition has already begun. It is also evident that IPv4 and IPv6 networks will need to coexist for some time during this transition.

Aligning Key Embedded Building Blocks

Meanwhile, there is another half to

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Figure 2

Layer 3 switch/router cards that allow wirespeed IPv4 and IPv6 forwarding are becoming available. For example, Curtiss-Wright's 6U 1/10 Gigabit Ethernet VME-682 FireBlade provides up to 24x 1 GbE ports and 2x 10 GbE ports of wirespeed IPv4/v6 performance in a single VME slot.

the equation: Are embedded platform networks in the battlefield also being transformed to support network-centric IPv4/IPv6 communications? Exploring their architectures, including the essential hardware and software building blocks, reveals indications that the transition to IPv4/v6 within embedded platform networks has already begun.

There is a multi-vendor ecosystem of building blocks, the members of which need to become aligned in order to support smooth IPv4 and IPv6 operation in an embedded system (Figure 1). For example, application developers need to write network-centric IP-based applications. RTOS vendors need to provide an OS with an integrated dual IPv4/v6 stack. Board vendors need to provide hardware with a board support package (BSP) and software drivers optimized for IPv4/IPv6-enabled hardware. In addition, backplane vendors need to provide standard and/or custom backplanes that enable systems integrators to build subsystems with switched architectures.

Software and Hardware Evolves to Meet IP Network Needs

The RTOSs used in embedded military systems have evolved over the years from a simple kernel and scheduler to a more complete solution that includes TCP/IP networking stacks. Although IPv4 integration within an RTOS has existed for several years, many RTOS vendors are now including dual IPv4/v6 stacks.

For example, for some time Wind River Systems has offered a separate IPv6 protocol add-on for VxWorks. More recently, a dual IPv4/v6 stack now ships standard with VxWorks releases versions 6.0 and up. Wind River's own tests of its dual IPv4/v6 stack on a PowerPC 8560 reference board have shown near-line-rate performance for both IPv4 and IPv6 forwarding over various packet sizes. This test confirms that a huge performance hit does not result from forwarding IPv6 packets (128-bit address size), compared to IPv4 packets (32-bit address size), on newer processors and protocol-optimized Gigabit Ethernet (GbE) controllers.

Similarly, embedded Linux, which is gaining momentum in embedded military/aerospace applications, has fully integrated IPv4/IPv6 capability. Other key RTOSs, such as Green Hills Software's INTEGRITY and LynuxWorks' LynxOS, also have direct or partnered IPv4/v6 solutions.

Many hardware vendors targeting the military have also begun to support dual-stack versions of IPv4/IPv6 via optimized drivers for specific RTOSs. In addition, an increased amount of Layer 3 switch/router cards that allow wirespeed IPv4 and IPv6 forwarding have come to market.

For example, Curtiss-Wright Controls Embedded Computing provides a complete set of 6U VME and 3U CompactPCI SBCs and multi-layer switches with dual IPv4 and IPv6 forwarding support, such as the 6U 1/10 Gigabit Ethernet VME-682 FireBlade, a managed Layer 2/3 switch/router (Figure 2).

Backplanes and the Formation of Network-Centric Platform Architectures

Efficient network-centric IP-based communications requires switched network architectures. Consequently, subsystem architectures have shifted recently from purely parallel bus-based architectures to switched architectures. Some of the key reasons for this shift include the ability to implement peer-to-peer communication, better overall performance, non-blocking operation and more flexible network topologies. All of these are required to create an efficient transport infrastructure that can carry IP packets within the embedded platform network.

For example, many system integrators are still developing or upgrading subsystems using VMEbus. To upgrade these legacy systems so they can support high-performance switched networks that efficiently transport IPv4 and IPv6 packets, one cost-effective approach is introducing a multi-layer GbE switch (Figure 3).

This approach can yield the maximum amount of reuse while transforming a legacy system into a high-performance switched solution. Common network topologies, such as centralized star or dual-star (redundant) network topologies, can be enabled by wiring up Ethernet ports from each processing blade in a chassis. This can be done by using a VITA 31.1 standards-based approach or by simply inserting a VME64-compatible switch card and wiring up an application-specific backplane.

The primary use for switched networks depends on the application. For moderate-performance applications, a standard switched GbE network can be used to transport control, management and data packets over TCP/IP (connection-oriented) or UDP/IP (connectionless). TCP Offload Engines (TOEs), Remote Direct Memory Access (RDMA) and kernel bypass techniques can be used to achieve better performance for higher-performance applications. At the same time, the use of standards-based Internet protocols or a lightweight protocol can be used for either loosely coupled or tightly coupled blade-to-blade communications.

Designers of other applications, such as radar and sonar processing, may find a combination of switched fabrics to be a better fit. The switched GbE network can still be used for blade-to-blade control, management and the monitoring plane within the box. A separate

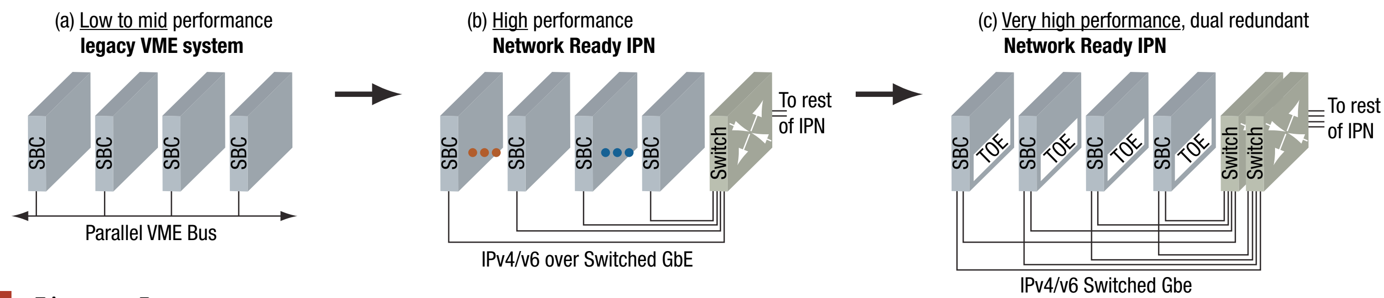

Figure 3

Upgrading a legacy VME subsystem to a switched IP network (IPN) can be accomplished in several different ways, depending on performance needs. These include introducing a multi-layer Gigabit Ethernet (GbE) switch and using a TCP Offload Engine (TOE).

high-performance fabric—such as Serial RapidIO (SRIO), PCI Express (PCIe), Advanced Switching Interconnect (ASI) or 10 GbE—can be used as the heavy data movement dataplane.

VME64 connectors can handle the 1.25 GHz signaling speeds of switched GbE in the backplane. However, they cannot handle the higher-frequency signaling speeds required by the higher-performance switched fabrics demanded in high-performance cluster computing. For example, PCIe and ASI serial switched fabric technologies require 2.5 GHz signaling, while SRIO and 10 GbE XAUI require 3.125 GHz. None of these fabrics are suited for routing through VME64 connectors.

However, new design architectures will soon be possible with the next-generation VPX (VITA 46) standard, expected to be finalized later this year. In a VPX system, it will be possible to use switched GbE for transporting IPv4/v6 packets to each blade for control, management and monitoring, along with a high-performance switched fabric for heavy blade-to-blade data movement.

In all of these cases, any remaining switched GbE interfaces can be used to address box-to-box internetworking. Boxes with GbE switches can be used to connect subsystems within a platform in a star, dual star, mesh or hybrid topology. Either 1 GbE or aggregated multiples of 1 GbE—or even 10 GbE, if supported—can be used as the box-to-box interconnect to create a system-wide intra-platform network.

The Move to IPv6

This underlying shift from parallel buses to switched intra-platform network architectures is one of the fundamental transformations required to enable efficient IPv4/v6 network-centric communications. The transformation has already started in VME systems with the introduction of switched GbE. It will continue to evolve with centralized and distributed switched architectures in upcoming VPX systems.

The transformation to network-ready IPv4/IPv6-enabled embedded systems within platforms has clearly begun at the lower layers. These embedded building blocks include RTOSs that now come integrated with dual IPv4/v6 stacks, hardware with optimized network drivers to complete protocol offload solutions and backplane solutions that can facilitate switched GbE networks today with a plan to support high-performance serial switched fabrics in the near future.

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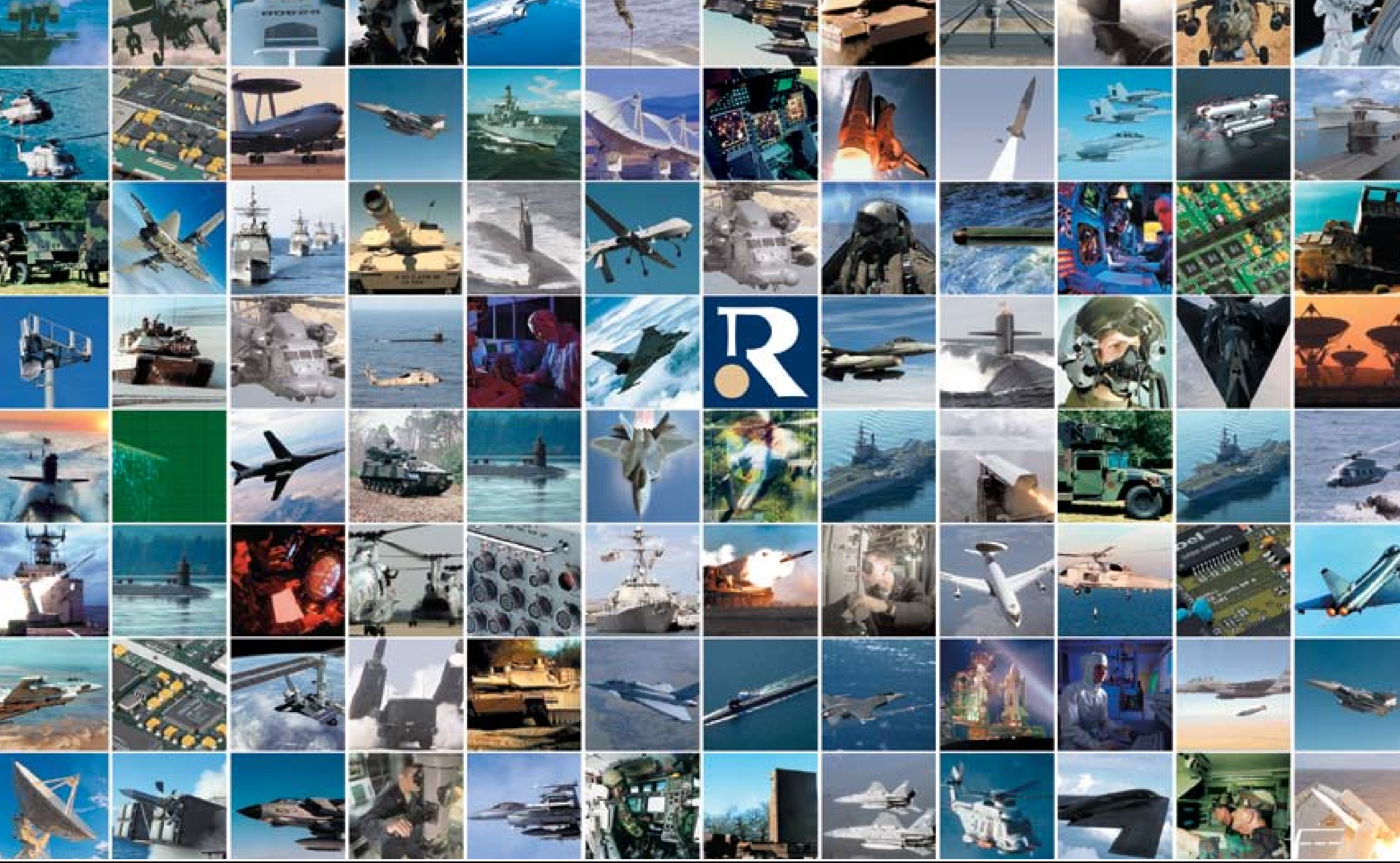

FPGA-Based SDR Platforms Ease Military Comms Challenges

The steady advance of Software Defined Radio technologies has enabled a wealth of ready-made platforms suited for next-gen military communications programs such as JTRS.

Nick Garnett, Field Applications Engineer
Spectrum Signal Processing

Few technology areas can claim as strong a synergy across the commercial and defense marketplaces as software defined radio. Military communication providers are reaping the benefits of that synergy. Software defined radio (SDR) is defined as a "collection of hardware and software technologies that enable reconfigurable system architectures for wireless networks and user terminals." SDR provides an efficient and comparatively inexpensive solution to the problem of building multi-mode, multi-band, multi-functional wireless devices that can be enhanced using software upgrades.

Military and defense communications providers can benefit from SDR systems that allow a platform's functions, modes and applications to be configured and reconfigured by software alone. SDR enables the use of one hardware platform for multiple applications. This allows system developers to spread their investment across multiple programs, thereby reducing project costs and mitigating technology risks by building foundational knowledge.

SDRs also allow the reuse of waveform code from platform to platform, which requires a software infrastructure supporting code portability. An example of this is the DoD's Joint Tactical Radio System (JTRS) program (Figure 1) that mandates future radios become interoperable, that is, support the different waveforms of its armed forces.

SDR technology eases the porting of applications to future hardware. This is important in the defense sector where applications can be deployed for a long period

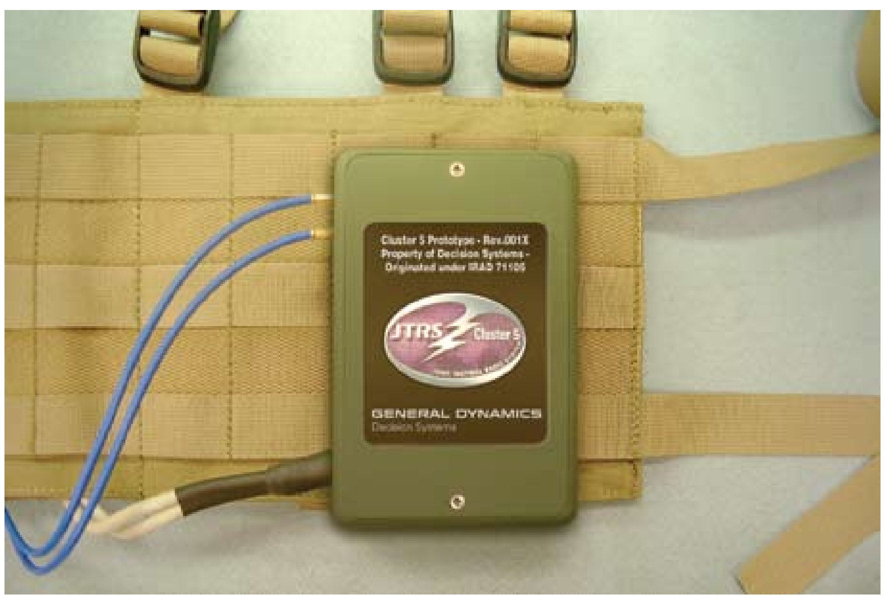

Figure 1

SDRs allow the reuse of waveform code from platform to platform, which requires a software infrastructure supporting code portability. This is important for the DoD's Joint Tactical Radio System program, which mandates future radios become interoperable, that is, support the different waveforms of its armed forces. The prototype shown here of a JTRS Custer 5 radio represents one of several radio sets or form-factors that could be called for under the JTRS program. In a recent reorganization of the JTRS program, Cluster 5 radios were renamed Handheld/Manpack/Small Form Fit (HMS) radios.

of time, which may extend beyond the lifetime of the hardware. These types of applications can include communication gateways, ground terminals for the Common Data Link (CDL) system and JTRS radios.

Programmable Hardware Infrastructure

Selecting the type of processing technology will be based on the requirements of an application and can include application-specific integrated circuits (ASICs), digital signal processors (DSPs), general-purpose processors (GPPs) and/or field programmable gate arrays (FPGAs). Military communications applications are increasingly required to fill multiple roles and support multiple modes of operation, usually dynamically and often simultaneously. As such, fixed function hardware components, such as ASICs, are efficient in traditional single-purpose applications but have limited use in SDRs. SDRs more frequently use reconfigurable components, such as DSPs, GPPs and FGPAs. Advances in FPGAs in particular, with its increased device capacity and speed, along with enhanced digital signal processor architectural enhancements, have contributed to the development of SDR technology.

Heterogeneous Processing

Platforms that combine the processing technologies of FPGAs, GPPs and DSPs are sometimes referred to as heterogeneous processing. The use of heterogeneous processing platforms offers a greater degree of flexibility to handle multiple missions and multiple roles.

A number of critical factors should be considered when designing the hardware and software infrastructure that employs heterogeneous computing boards. Typical computer buses, such as PCI, dramatically limit the ability to feed data to and consume data from processing devices, especially when the bus is shared. Designing dedicated high-speed point-to-point data links that provide deterministic low-latency data flow can solve this problem. Switched fabric protocols, such as Serial RapidIO, are ideal for implementing inter-processor and inter-board interconnects.

Developing consistent and effective interfaces between various processing devices and to elements external to the processing

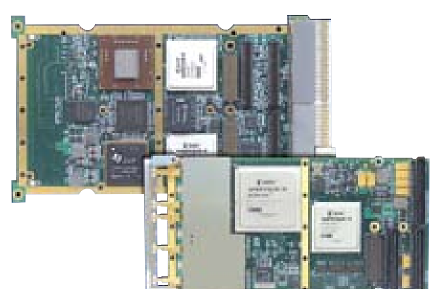

Figure 2

Embedded computing platforms are available that provide necessary SDR hardware and software infrastructure. An example is Spectrum Signal Processing's flexComm SDR-4000. The SDR-4000 includes two major component-level products: the PRO-4600 SDR heterogeneous processing engine and the XMC-3321 dual transceiver input/output XMC mezzanine card.

is difficult. For example, loading FPGA cores requires specialized interfaces, however, contemporary operating systems and typical board support packages do not provide adequate provision for using FPGAs or DSPs. An integrated board and system-level software infrastructure are required to resolve these issues.

Partially Reconfigurable Processing Resources

Some SDRs may utilize a "shared resource" processing model where waveform components from two independent waveforms run on a single signal processing device. This is done to maximize the processing capacity of the overall system (the cumulative excess processing capacity may be enough to support additional channels). For these systems, processing resources must be capable of being partially reconfigurable.

In partial reconfiguration, already allocated processing resources must continue operating while other resources are allocated, loaded and started. GPPs are partially reconfigurable by nature of their operating system, while DSPs are only partially reconfigurable if an operating environment is provided that accommodates this functionality. However, the capability to support partial reconfiguration in FPGAs is relatively new and is not widely offered yet.

Previous generations of FPGAs require the entire contents of the FPGA to be reloaded in order to change any part of the core. Partially reconfigurable FPGAs are designed to allow implementation of FPGA modules that can be independently loaded and unloaded while other modules continue to operate. This requires mechanisms to not only retain the operating modules, but also the logic that interconnects modules that continue to operate.

Many of the applications that need to run on an SDR require very high throughput, deterministic low-latency operation and connections between processing devices. Switched fabric technologies, such as Serial RapidIO, provide these capabilities, however, supporting one type of fabric protocol may not be sufficient. Existing system components may support one or more fabrics other than a board's fixed fabric interface. Implementing fabric interfaces in FPGAs allows the fabric protocols to be reconfigured by simply loading a core that supports the needed fabric protocol stack.

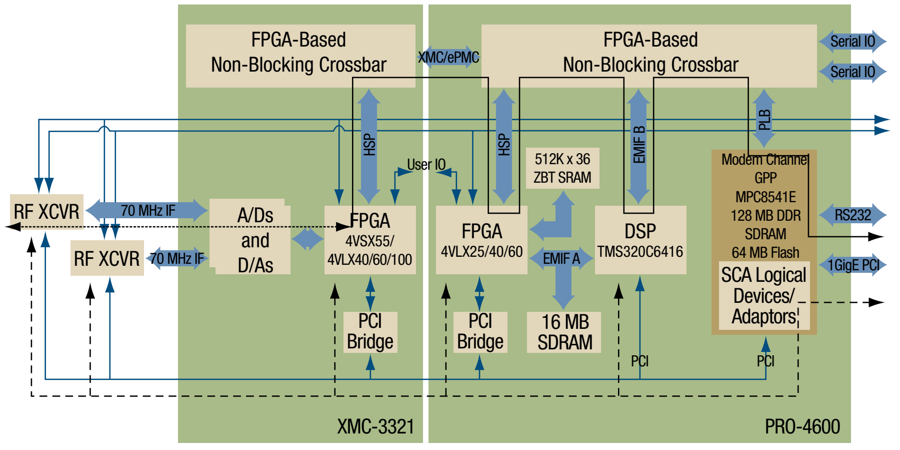

Figure 3

This block diagram of the SDR-4000 depicts the data flow between the processing engine and the transceiver. The two boards in combination provide two Virtex-4 FPGAs, a TI C6416 DSP and a Freescale MPC8541E PowerQUICC III GPP. High-speed dedicated point-to-point data links are provided between the two boards. Processing elements on the host card are interconnected for data via an FPGA-based crossbar that provides high-speed point-to-point data links to the processing elements on the board, to the XMC interface and to the backplane.

Software Infrastructure: Operating Environment

The foundation of an SDR is the system's Operating Environment (OE). The OE is much more than just an operating system and requires more integrated functionality than provided by most board support packages. The OE provides application program interfaces (APIs) for operating system call access, loading and linking software components, configuring and operating hardware and software and setting up and operating multi-segment data links.

In some programs, such as JTRS, the operating environment provides middleware and additional libraries that applications must use to be isolated from system calls that are unique to particular operating systems. One key component inside the JTRS program is the use of the open-standards Software Communications Architecture (SCA).

One of the challenges in systems with heterogeneous processing components is getting the different types of processing devices to interface with each other, whether they are on a single board or different boards. To be effective, an OE must provide a mechanism for abstracting connections and hiding the underlying mechanism from the applications developer. This is done by providing an identifier or name for data destinations along with protocols for routing data from the source to the identified destination.

In TCP/IP connectivity, Internet addresses, domain names, packet protocols, socket-based APIs and network routing protocols fill these roles. An effective OE implements each of these abstractions. Each processing element is assigned an identifier that is unique within the system. For systems with a small number of possible hops between source and destination processing element, links are most efficiently implemented using a packet header that provides the unique identifiers for the source, destination and all intermediate interfaces.

Domain Management and Profile

For SDRs that need to support code portability, human-readable and editable files are required to provide descriptive and configuration data for all hardware and software components in the system. These files, collectively known as the domain profile, are read and parsed by a domain manager software component. The domain manager uses the profile data to allocate hardware and software resources for given applications, configure all hardware and software components and support maintenance of the dynamic status of the entire system.

Component-based software in an SDR can ease application development and improve code portability. Component-based software is composed of operationally related functions that are linked into a single load module, which can be loaded independently of other load modules and can communicate with other software components via middleware or operating system component communication mechanisms.

The earlier discussion on a shared resource processing model and partial reconfiguration has impact on the software infrastructure as well as the hardware infrastructure. The OE for a system that supports partial reconfiguration in a heterogeneous computing board must provide services to load and unload FPGA modules to specific groups of FPGA logic cells, consistent with the FPGA's partial reconfiguration mechanism.

Real-World Example

Software defined radio is becoming a reality in today's military and defense applications. An example of a software defined radio platform with the necessary SDR hardware and software infrastructure is Spectrum Signal Processing's flexComm SDR-4000 (Figure 2). The SDR-4000 includes two major component-level products: the PRO-4600 SDR heterogeneous processing engine and the XMC-3321 dual transceiver input/output XMC mezzanine card. Figure 3 is a block diagram of the SDR-4000 depicting the data flow between the processing engine and the transceiver.

The two boards in combination provide two Xilinx Virtex-4 FPGAs, a Texas Instrument C6416 DSP and a Freescale MPC8541E PowerQUICC III GPP. The boards also provide high-speed dedicated point-to-point data links between the two boards. Processing elements on the host card are interconnected for data via an FPGA-based crossbar that provides high-speed point-to-point data links to the processing elements on the board, to the XMC interface and to the backplane.

The SDR-4000 uses Spectrum's quicComm, a high-performance hardware abstraction layer and software library, for its operating environment. The quicComm library facilitates the implementation of complex signal processing and data acquisition applications by abstracting low-level details, allowing the programmer to focus on their signal processing application. The quicComm library includes support for high-performance inter-processor communications hardware and other board-level features such as interrupt handling. The API is designed to be simple and user friendly, isolating the programmer from the complexities of the hardware while maintaining near-hardware-level performance.

Software defined radios have the capabilities to meet the multi-role, multimode and multi-function requirements of military communications applications and requires the right hardware and software infrastructure to realize the benefits of this advanced technology. ▮

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FPGAs Edge Out GPPs for Advanced Signal Processing Apps

General-purpose processors (GPPs) suffer an inherent imbalance between I/O and processing. FPGA-based processing is emerging as a better alternative for signal processing chores such as advanced radar designs.

Bob Walsh, Field Applications Engineer
TEK Microsystems

Signal processing systems today use FPGA-based processors to perform processing at higher densities than is possible with general-purpose processors. The use of the same tools and techniques supports a scalable and flexible approach to building signal processing systems.

Leveraging off-the-shelf hardware and software, along with tailoring when necessary through FPGA-based processing, allows the use of industry standard components, enclosures, backplanes, I/O modules and RAID disk arrays. This makes it possible to develop very high-performance signal processing systems with application-specific tailoring where necessary while reusing existing hardware, software and FPGA components for the majority of the system.

By connecting multiple FPGAs on a board or across boards over the backplane, military system developers can craft extremely powerful processing machines for applications such as image processing and advanced radar processing. An example is the next-generation radar system being developed for the E-2D Advanced Hawkeye (Figure 1).

General-Purpose Processors Found Lacking

The biggest drawback with general-purpose processors (GPPs) is the imbalance between I/O and processing. There is only one path to and from main memory. The processor can perform complex calculations faster than it can fetch operands or store results. Thus, many algorithms are I/O bound, limited by the access speed rather than the calculation times.

Advanced processors with on-chip caches can do better, but only if the next operand is already in the cache. Often it is not, so the operation stalls while it is fetched. These processors work best on problems that have a high ratio of processing steps to I/O points, like long FFTs. General-purpose processors such as the Altivec aren't a good solution for a FIR filter, since each input point is used in just a few calculations. The processor spends most of its time waiting for the memory interface.

Field Programmable Gate Arrays (FPGAs) can provide more efficient solutions to embedded signal processing problems. FPGAs are very fast, and very flexible, and are available at an intermediate cost. FPGA solutions are designed at the gate level, but using a programming language such at VHDL or Verilog makes accessing their power easier than when a wire wrap gun was used 20 years ago. FPGAs don't have a single "CPU" like a microprocessor does; the designer can use the chip's resources to build whatever architecture is appropriate for the problem at hand. FPGAs have a much better balance between processing power and I/O capability.

Many Processing Chains

If, for the sake of application efficiency, it makes sense to have a large

Advanced Hawkeye Configuration

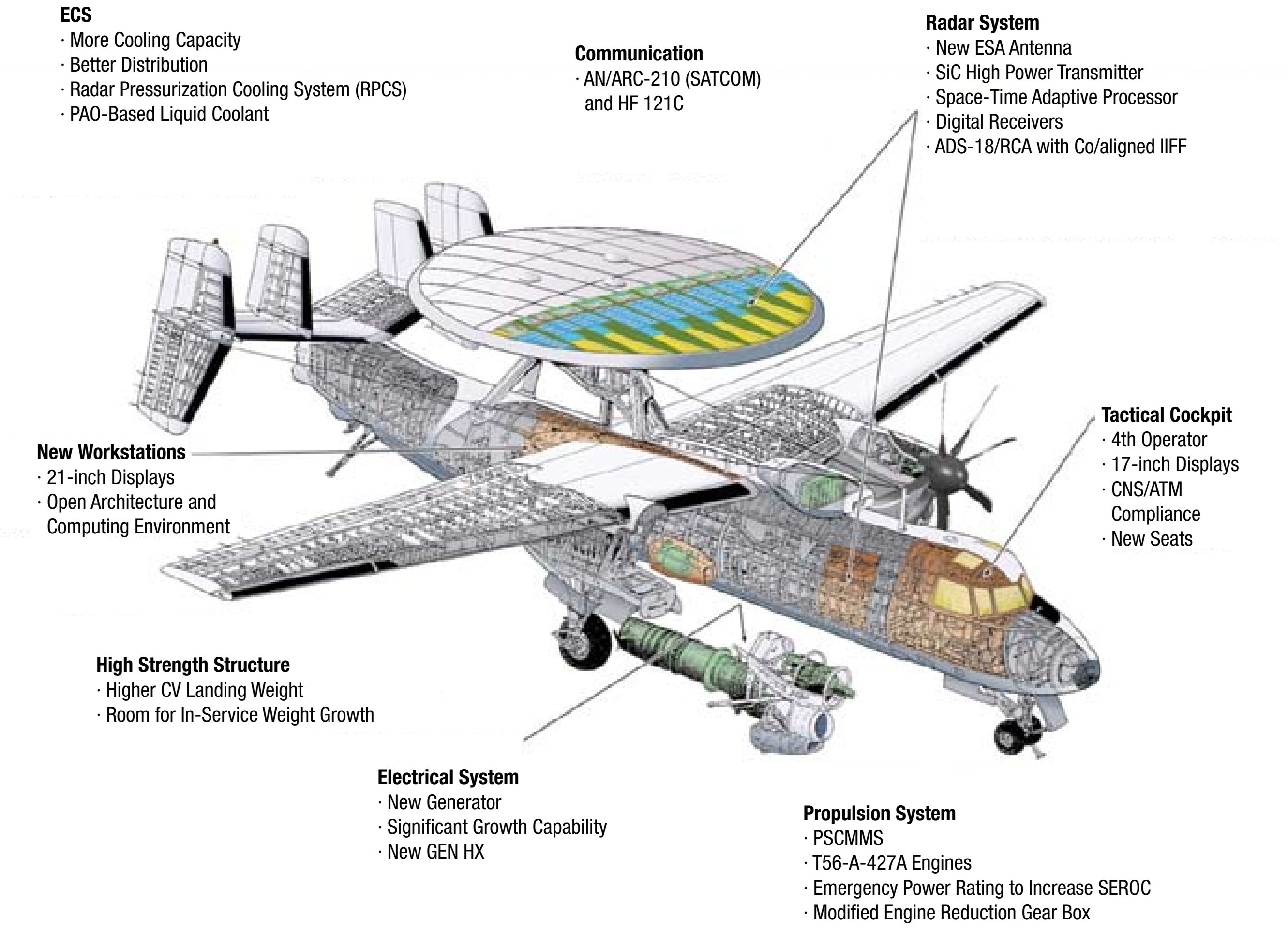

Figure 1

The next-generation E-2D Advanced Hawkeye aircraft will be the U.S. Navy's next-generation airborne early warning and battle management system. The E-2D Advanced Hawkeye will be the latest version of the Hawkeye family of aircraft and will feature a new radar system along with other advanced capabilities, relying on FPGA-based protocol engines to support application-specific processing in real time during record and playback.

number of simple processing chains running in parallel, that can be easily implemented. An FPGA can do FIR filtering much more efficiently than a general-purpose microprocessor by implementing a large number of filters that operate in parallel. Alternately, if the problem demands more complex processing, those calculations can be done in fixed point, which saves time and resources in the FPGA. Also, the designer is not limited to a fixed word size. The architecture can be tailored to the problem at hand.

The "field programmable" part of FPGAs means that a standard hardware design can perform a variety of functions in the fielded product, since the functionality is determined by the bit stream that is loaded at power-up time. The hardware functionality is completely determined

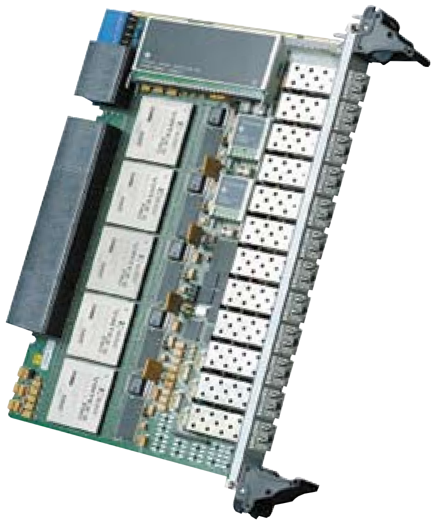

Figure 2

The FPGAs on the Callisto switch card can be programmed to handle processing tasks more efficiently than general-purpose processors.

by the software that is loaded onto it. This flexibility comes at a price: designing and debugging complex FPGA designs can be difficult.

The designer is working at a lower level than with a general-purpose processor, which adds a layer of complexity to the design and checkout work. Fortunately simulators are much more powerful today than in the past, and many problems can be discovered before actually programming a chip. And with FPGAs, fixing an error is done in software; we don't have to throw away any defective hardware.

FPGA Implementation

It's not enough to glue an FPGA to a board to have an efficient system. To get the full benefit of FPGA technology,

Figure 3

Using the Virtex-II Pro FPGA, a complete data recording system is now available as a system-on-a-chip (SoC).

high-speed interconnects are required between individual FPGAs, auxiliary RAM, and a complete I/O system. For example, the Callisto FPGA processing board designed by QineitQ RTES in the UK includes five Xilinx XC2VP20 or XC2VP50 Virtex-II Pro FPGAs (Figure 2). Each FPGA has a 128 Mbytes of DDR SDRAM associated with it, configured as 16 bits by 64 Mwords. The DDR RAM provides buffer storage for applications like SAR corner turns.

The five FPGAs on the board are connected with a 2x 64-bit-wide parallel bus that can support full duplex data rates above 1.5 Gbytes/s. Next, the FPGAs are connected to 4x serial connections over the VXS backplane that run at 3.125 Gbits/s each. Each FPGA has three or four 4x connections, for a maximum of sixteen for the entire board. The board also includes twelve Small Form Pluggable (SFP) connections on the front panel, for fiber or copper serial connections that run at 2.5 Gbits/s.

Callisto fits in the "switch" slot in a VXS backplane, and has an enormous amount of backplane I/O available to it—approximately 20 Gbytes/s total. The front panel connections provide another 3 Gbytes/s. The Virtex-II Pro FPGAs could be programmed with switching cores and act as a traditional switch. But a more innovative use of the board is to program the FPGAs as processing nodes, and use the I/O lines to bring input data to the system from "payload" cards.

An even more interesting use connects multiple boards to each other over the backplane. An interconnect scheme can be designed that connects the FPGAs on several boards into a mesh architecture. This would result in the ability to build an enormously powerful processing machine for applications such as image processing.

The Virtex-II Pro FPGA includes a general-purpose processor (PowerPC) core along with the array of logic gates. This allows the designer to use the PowerPC for tasks that it is well suited for, while still having all the advantages of the gate array. For instance, this functionality could be used to implement a complete Fibre Channel data recorder function on the board with no additional hardware. This would allow a simple data recorder function to be added to a system without having to use dedicated disk controller hardware (Figure 3).

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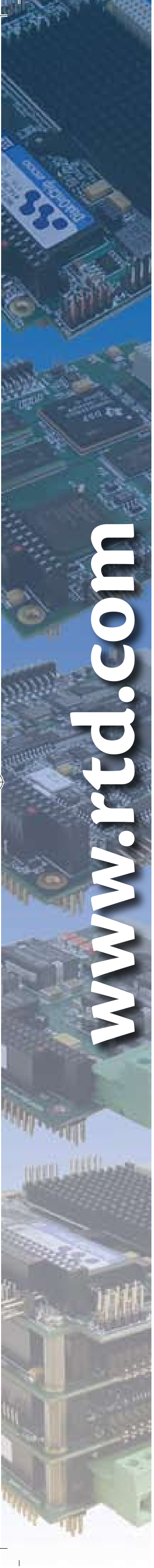

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Bus	AT Expansion Bus					✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓		
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4		4	4		
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9					
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1000	1000	650	650	650	650	650	650	333	333	333	100	100
	L2 Cache	2MB	2MB	512k	512k	256k	256k	256k	256k	256k	256k	16K	16k	16k	16k	16k
	Intel SpeedStep Technology	✓	✓													
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0					
	Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	512	512	256	256	256	32	32
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Fail Safe Boot ROM					✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓					
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
	SSD Socket, 32 DIP						1		1		1	1	1		2	1
	ATA/IDE Disk Socket, 32 DIP	1	1	1	1	1		1		1				1		
	Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓					
	Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	TTL		
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA		
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
I/O	RS-232/422/485 Ports	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	USB 2.0 Ports	2	4	2	4											
	USB Ports					2	2	2	2	2	2	2	2	2		
	10/100Base-T Ethernet	1		1		1	1	1	1	1	1	1	1	1		
	ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO(Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18		
	multiPort(aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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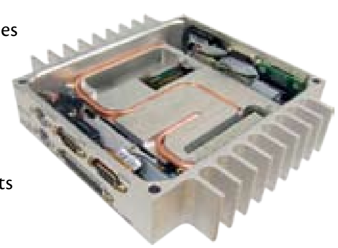

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Bus	AT Expansion Bus	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master	✓	✓				✓							✓
	McBSP Serial Ports	✓	✓				✓							
Analog Input	Single-Ended Inputs	16	16	16	16	16	16							
	Differential Inputs	8	8		8	8	8							
	Max Throughput (kHz)	1250	1250	40	500	100	1250							
	Max Resolution (bits)	12	12	12	12	16	12							
	Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6							
	Autonomous SmartCal	✓	✓											
	Data Marker Inputs	3	3		3		3							
Conversions	Channel-Gain Table	8k	8k		8k	8k	8k							
	Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓							
	A/D FIFO Buffer	8k	8k		8k	8k	8k							
	Sample Counter	✓	✓		✓	✓	✓							
	DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓						✓
	SyncBus	✓	✓				✓							
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48
	Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48
	Advanced Interrupts	2	2		2	2	2	2	2					2
	Input FIFO Buffer	8k	8k		8k	8k	8k							4M
	Opto-Isolated Inputs										16	48	16	
	Opto-Isolated Outputs										16	16		
	User Timer/Counters	3	3	3	2	3	3	3	3	3				10
	External Trigger	✓	✓		✓	✓	✓	✓	✓					✓
	Incr. Encoder/PWM									3/9				
	Relay Outputs												16	
Analog Out	Analog Outputs	2	2		2	2	2	4						
	Max Throughput (kHz)	200	200		200	100	200	200						
	Resolution (bits)	12	12		12	16	12	12						
	Output Ranges	4	4		3	1	4	4						
	D/A FIFO Buffer	8k	8k				8k	8k						

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Military Simulation Rides Wave of Gaming Graphics Innovations

Gaming graphics and military simulation enjoy a long history with each other. New PC graphics processors are enabling more realism and performance.

Simon Collins, Graphics Product Manager
Radstone Embedded Computing

The link between graphics in military simulation applications and commercial/consumer gaming technologies and applications goes back many decades. The most significant breakthrough in that relationship occurred with the advent of power PC graphics technologies powerful enough to serve the needs of military simulation applications.

In the late 1990s, the U.S. Army PEO STRI (Program Executive Office for Simulation, Training and Instrumentation) began to evaluate Windows-based PCs as a possible replacement for SIMNET's aging hardware, compelled by the increasing capability of PC graphics hardware and the growing availability of commercially available IGs (Image Generators). Equally compelling was that repair of the GT-111 hardware at the heart of SIMNET was becoming close to impossible, with individual boards costing over $4,000 to fix. (See sidebar "Gaming and Military Simulation Share a Long History Together" for more information about the earlier bonds shared between the entertainment gaming industry and the military simulation realm.)

At around that time, the nVidia RIVA 128 graphics card featured 3.5 million transistors, a clock speed of 100 MHz, a single pixel pipeline and the ability to deliver 100 million texels. A texel, or texture element, is the fundamental unit of texture space used in computer graphics. Textures are represented by arrays of texels, just as pictures are represented by

Figure 1

Developed by Radstone subsidiary Octec, the SIVET provides operator training for the Royal Navy's Type 23 Frigate Automated Small Calibre Gun System. Shown here, the Type 23 Frigate HMS Richmond provides naval gunfire support for Commando forces ashore.

GPU Performance 1997 - 2006

	nVidia RIVA 128	nVidia GeForce 7800GT	Improvement
Transistors	3.5 million	302 million	86x
Clock Speed	100 MHz	400 MHz	4x
Pixel pipeline	1	20	20x
Texels	100 million	8,000 million	80x

Table 1

In less than 10 years, the graphics processing capabilities have enjoyed dramatic increases, with texels ramping up at around the same rate as the number of transistors per chip.

arrays of pixels) per second. The nVidia GeForce, by comparison, has 302 million transistors, a clock speed of 400 MHz, twenty pixel pipelines and is capable of 8,000 MTexels/s (Table 1). The PEO STRI was highly prescient in its analysis of the opportunity for continuing systems enhancement at lower cost; it seems as if a new graphics card from ATI or nVidia is announced every couple of months.

The nVidia GeForce graphics processor is used in the SIVET (Simulated Infrared/Visible Engagements with Targets), which provides operator training for the Royal Navy's Type 23 Frigate (Figure 1) Automated Small Calibre Gun System to be supplied by MSI. It produces real-time video sequences that include complex, dynamic backgrounds and multiple, independent objects that interact with the background, and can also be used to evaluate closed-loop Automatic Video Tracking (AVT) of various targets by various dynamic platforms. Although land-based in the near term, ruggedization would allow its deployment onboard ship.

Quest for More Realism

Of course, what has always driven the PC graphics card industry has been the quest for ever-greater realism—a more convincing, more immersive, more satisfying game-playing experience. For the designers of military simulation systems, the requirement is no different: the more real the simulation, the more engaging it is—and the more realistic its outputs and outcomes will be.

Developers of military simulation systems should bear in mind that an increasing number of the personnel who will interact with their systems will have grown up with PC-based games—with their astonishingly high-quality graphics. Top-end graphics cards costing several hundred dollars are designed exclusively for serious gamers, and water-cooling is becoming increasingly popular to dissipate the heat they generate. Meanwhile, their quest continues for a level of realism that approaches photographic quality. Those who have enjoyed these games are unlikely to be compelled by a military simulation that is less true to life, nor is a less-than-adequate graphic simulation likely to inspire the necessary confidence. A term being more widely used in military simulation circles is "virtual reality"—perhaps the ultimate in simulation.

If there is a growing trend in defense simulation applications to borrow extensively from the hardware and software technology that enable PC gaming, there is an equally observable trend for simulation to move from a classroom or operations room at headquarters to deployed platforms. The thinking is that this allows either training to take place during periods of inactivity (thus minimizing "downtime") or that the situation surrounding the deployed platform can be simulated, and appropriate strategies devised, prior to any of its occupants exposing themselves to danger.

The implications of this trend are twofold. First, a new type of simulation hardware is required that is not only compatible (in terms of performance, form-factor and ruggedness) with existing in-vehicle hardware—it may

Gaming and Military Simulation Share a Long History Together

The worlds of entertainment games and military simulation share a common technology link that can be traced back across several decades. Consider for example, Edwin Link, who developed the first pilot training simulator. While waiting for the Navy to sign contracts for it, he sold the trainer to amusement parks—the worlds of entertainment and military simulation were already inextricably linked.

Since then it was developments in computing that dominated the relationship—and that have driven simulation technology to become a major strategic asset for the United States, with investment far outstripping that of other countries. By the 1980s, the U.S. Army was evaluating—and modifying—Atari's "Battlezone" FPS (first person shooter) console game, to give it controls that better resembled those of a Bradley infantry fighting vehicle, with a view to improving soldier hand/eye coordination. Early in the same decade, the U.S. Navy was looking at the possibilities offered by Microsoft's Flight Simulator—and found that students who used it during early training tended to have higher scores than those who did not.

Perhaps the most important development in computer-based simulation was that of SIMNET (SIMulation NETwork) by DARPA in the late 1980s—an array of individual simulators connected together. With its limited visual range of a little over two miles, screen resolutions of 320 x 240 pixels and a refresh rate of only fifteen frames/second, SIMNET seems impossibly limited today—but was representative of the state of the art at the time.

Then in the late 1990s the link with PC graphics and military simulation became solid when the U.S. Army PEO STRI (Program Executive Office for Simulation, Training and Instrumentation) began to evaluate Windows-based PCs as a possible replacement for SIMNET's aging hardware. The decision was compelled by the increasing capability of PC graphics hardware and the growing availability of commercially available IGs (Image Generators).

even be the same hardware, adapted for both operational and simulation purposes, thus saving the precious space and weight that are becoming increasingly constrained in today's operational platforms.

A key feature of Radstone's Screaming Eagle board (Figure 2) is that it is implemented in the 6U VME form-factor, allowing it to make use of available chassis/enclosure space, rather than requiring additional housing. Second, there is an obvious requirement that these new simulation systems deployed in harsh environments—such as tanks—should be rugged, capable of withstanding shock, vibration and extremes of temperature. Radstone's roadmap for Screaming Eagle sees the availability of a rugged variant that will respond to precisely this requirement. The Screaming Eagle, which sports an nVidia GeForce GPU, is at the heart of the SIVET embedded training subsystem mentioned earlier.

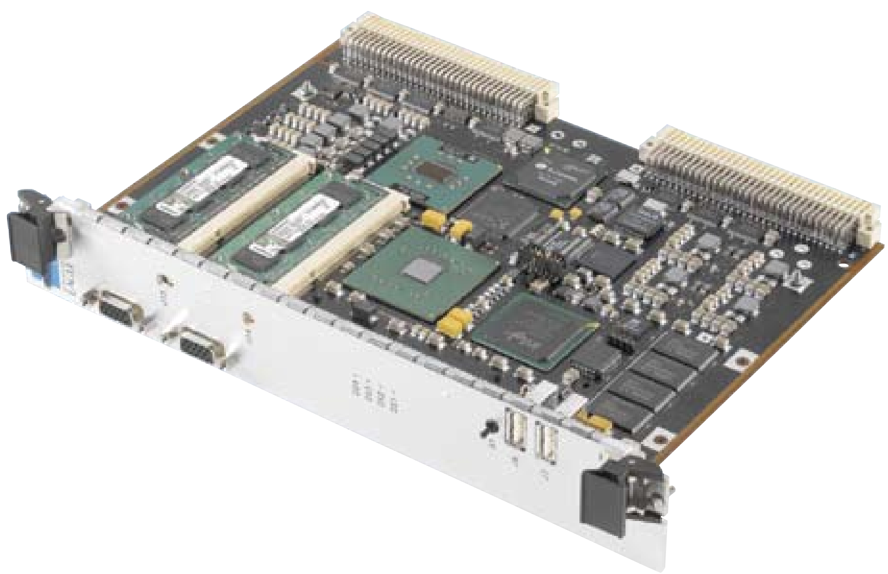

Figure 2

Radstone's Screaming Eagle graphics board features a GPU more commonly found in PC-gaming platforms

Embedded Simulation Trend

One of the most notable deployed platforms to feature embedded simulation/training is the Bradley Fighting Vehicle. Its onboard capability allows troops, for example, to rehearse planned maneuvers while the vehicle in which the maneuver will be executed is being transported to the battlefield. Current thinking is that there is no reason why the graphics card that is at the heart of an onboard simulation system should not be the same graphics card that is responsible for processing and displaying "real-world" situational information—perhaps equipped with a simple switch enabling it to toggle between its simulation/training application and its primary application. In an ideal world, it could be said that the personnel would be unable to distinguish the images delivered by the two applications.

The quest for ultimate realism in simulation is an ongoing one, however—and if history is any guide, its future will be closely tied to that of the PC gaming industry. To understand where it might go in the future, it's important to understand what the GPU has brought to the party—and what it has not brought.

An important distinction that's made by game developers is the distinction between graphics on the one hand and physics on the other. Today's state of play has been reached, to a large extent, thanks to OpenGL. In the early days of computer graphics, the programmer was forced to individually code even the simplest routines—such as drawing a line, or filling a shape—often with reference to each individual pixel in the display. Time-consuming and tedious, the need for tools that would automate graphics functions rapidly became apparent. PHIGS (Programmer's Hierarchical Interactive Graphics System) was designed in the 1980s, and became an ANSI and ISO standard. By today's criteria, it was extremely basic—although it should be said that the then-available hardware was not capable of anything beyond basic graphics.

It was in 1992 that SGI (Silicon Graphics Incorporated) led the creation of the OpenGL standard, a standard based on the company's proprietary IrisGL API (Application Programming Interface) that was designed for its high-end graphics workstations. It had two key benefits. First, and unlike Microsoft's competitive product DirectX, it was portable across platforms. Second—and related to the first—was that it provided support in software for features that were not supported by the underlying hardware, allowing the development of sophisticated graphics applications on relatively unsophisticated hardware.

OpenGL Eases the Way

OpenGL brought with it a revolution in computer graphics, for two reasons. First, coding more complex, more realistic graphics applications became significantly easier to do; and second, increasing numbers of OpenGL routines were implemented in hardware by GPU manufacturers, allowing those applications to run in an optimum, highly accelerated environment.

But as noted previously, there is a distinction in PC game development between graphics and physics. The combination of OpenGL and increasingly powerful graphics processors has addressed the former, but not the latter. While graphics technology typically addresses the interaction of objects and surfaces with light, physics technology deals with the interaction of objects—both with their environment and with each other. Like graphics, it is possible to reduce this interaction to mathematical formulae and equations—and should therefore, in theory at least, be capable of being addressed by a similar combination of API and application-specific hardware.

Focus on Physics

Enter the PPU, or Physics Processing Unit. Designed to offload from the CPU calculations such as fluid dynamics, hair and clothing simulation, fracturing and other complex object interactions, it is specifically created to improve the level of realism in PC gaming—and, by implication, it will do the same for simulation applications. As with GPUs and OpenGL, a PPU would come complete with an API that would simplify and speed up the development of physics elements within games—and would also provide software support for routines not directly supported by the PPU itself.

The thinking is that the realism of today's games is inherently limited by the comparatively small number of objects that can interact—with each other, with their environment and even with the user/game player—simultaneously. An explosion, for example, cannot be accurately simulated because the motion and interaction of only a relatively few fragments can be reproduced in parallel. A PPU would, the thinking goes, allow the modeling of perhaps tens of thousands of individual objects in parallel.

Naysayers say that the PPU is a step too far—and that its utility will largely be negated by the increasing capabilities of today's CPUs. However, the fact that the idea is being mooted at all is indicative of the fact that there are many who see the quest for absolute realism—in other words, photo-quality realism becoming movie-quality realism—as being far from over.

Meaningful, productive simulation is, much like PC gaming, all about the ability to force the viewer/player to suspend disbelief, to become immersed in a world that is not real. Graphics in today's simulation applications are already at a level of realism that was unimaginable only a few years ago: the signs are that they will only get better. ■

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Multicore and Fabric Trends Invigorate VME SBCs

Jeff Child, Editor-in-Chief

If you asked anyone present 25 years ago on that historic fall day in New York City, when VME was introduced to the U.S. market, where VME would be a quarter-century later, I doubt any could have predicted the amazing success and longevity this bus architecture/form-factor has today achieved. VME has weathered a formidable number of technology and market hurdles over its lifetime, and still remains a leading embedded computing form-factor, and enjoys a huge installed base in numerous military programs.

It's interesting to contrast the latest and greatest VME single board computers in the Roundup section on the next six pages, to the ancient Motorola MVME101 SBC based on a 1 MHz 68000, with RS-232C and dual channel serial/parallel ports for I/O. Part of VME's ability to weather obsolescence woes is thanks to specialist companies such as GD California. It has created a business out of providing boards, like the MVME101 in Figure 1, which have been discontinued by their manufacturer, through a mix of end-of-life buys and using programmable devices to produce compatible products for many discontinued boards.

One unique trends that's coming together in VME SBCs, and in embedded computing in general for that matter, is the shift to dual-core processors. The road maps of the leading processors show that all roads lead to architectures sporting multiple CPU cores on the same device, and VME SBC designers are putting them on their boards—and not waiting for such processors to mature in the desktop market first. Many military applications have an immediate need for the level of computing muscle such devices provide. Compute-intensive applications such as sonar, radar, SIGINT and UAV control systems fall into that category, along with several others.

As the industry looks ahead to the next 25 years, VME has run out of ways to squeeze performance while remaining a strictly parallel-bus architectures. Serial switch fabrics have begun to take their place alongside, and in hybrid configurations with, parallel-backplane designs targeted for embedded computers in military applications. And while emerging VITA specs like VXS (VITA 41) and VPX (VITA 46) aim to blend fabrics into the VME universe, they foretell a definite move away from traditional parallel-bus schemes like VME64 and VME 2eSST.

Those specs are getting closer to ANSI standardization. In fact, the VXS specs 41.0, 41.1 and 41.2 have completed ANSI ballots and have been recognized as American National Standards. Final published copies will be available from the VITA office shortly. Meanwhile, VITA 46—or VPX as it is now referred to in marketing circles—aims to develop a 3U/6U 160 mm deep Eurocard module with a high-performance connector capable of supporting both parallel and serial fabrics. VITA 46.0 and 46.1 have been moved into the ANSI process. A related activity, VITA 42, also called XMC, aims to extend PMC to include serial fabrics. 42.0 is now in trial use through March 2007. 42.1 and 42.2 have been recognized by ANSI. The working group has voted to send 42.3 to the ANSI process.

As fabrics become a part of the VITA landscape, the question arises as to whether such hybrid or fully switched serial fabrics can truly be called VME. VITA is taking that in stride in its marketing efforts, by expressing the "V" in VITA as applying to more than just VME. For its part, Tundra Semiconductor, the main supplier of VME interface silicon, says it intends to follow the VITA roadmap with VME interface chip products. Tundra's Universe VME interface chips dominate the installed base of VME board products now deployed. Earlier this year, Tundra introduced the Tsi148, a PCI-X-to-VME bridge and just last year added an industrial version of that VME 2eSST-enabled bridge. ■

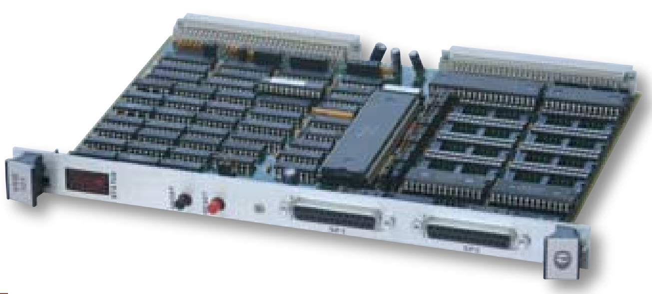

Figure 1

Illustrating what a long way VME has come, compare this Motorola MVME101 SBC based on a 1 MHz 68000—and through-hole DIP ICs—with RS-232C and dual channel serial/parallel ports for I/O, to the latest cutting-edge VME SBCs in the Product Roundup on the next several pages. Companies like GD California specialize in providing boards, like this MVME101, which have been discontinued by their manufacturer.

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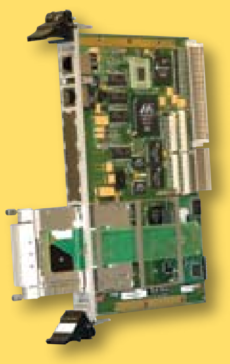
Technology Focus:

VME SBCs Roundup

PowerPC Board Features Hot Swap Storage

VME SBCs tend to get designed in for a long life cycle in military applications. But chances are good that its data storage will have to be swapped out frequently. Along just such lines, ACT/Technico's 5800 / 5801 series is a new high-performance VME SBC around the Freescale 1.7 GHz MPC7447/7448 PowerPC. The 5800 SBC can be shipped with a PMC-based, removable storage device, available in



standard and rugged grades up to 120 Gbytes. This low-power PowerPC design is available in standard and conduction-cooled versions, with operating temperatures between -40° to +75°C.

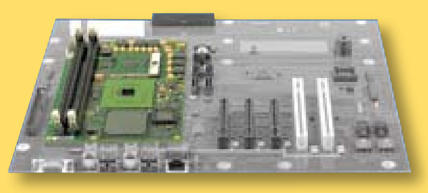
The 5800 is ideal for use in applications requiring high-performance processing. The VMEbus interface uses the 2eSST-compatible Tundra Tsi148 VME bridge and the latest TI transceivers. 2eSST can provide up to 300 Mbyte/s transfer rate across the VMEbus.

The board provides up to 1 Gbyte of SDRAM. A Marvell Discovery III chipset provides enhancements such as: data streaming on MPX bus, read memory latency and cache coherency improvements. The 5800 supports three Gbit Ethernet channels, one console port and one USB2 controller. A quad UART provides four additional asynchronous channels available on P2 connector. The 64-bit PCI/PCI-X bridge allows the VME SBC to control two PMCs. An optional 6U rear transition module adds two Gbit Ethernet RJ45s, USB2, four RS-232/422 ports, two SATA and 1 HD68 connectors. An engineering kit for debug is available. Operating systems supported are VxWorks and Linux. Onboard firmware includes Uboot, which provides power-on built-in test booting and remote software downloading over Ethernet.

ACT/Technico
Ivyland, PA.
(215) 957-9071.
[www.acttechnico.com].

SBC Boasts Distributed Dual-Processing Scheme

This year is shaping up to be the year of dual processing. Processor and board vendors alike are in the thick of the trend toward maximizing the effectiveness of multiple CPUs in a system. Offering a unique approach to dual-processing, Aitech Defense Systems offers a rugged 6U VME single-slot SBC that maximizes functionality and power by incorporating dual processors that operate independently of one another, yet communicate over a high-speed PCI-X interconnecting bus. The new C102's processors use an asymmetrical distributed architecture so that each of the processing nodes functions as a complete subsystem complete with local memory resources and basic I/O interfaces, eliminating data flow bottlenecks. The C102's improved processing power and I/O functionality make it ideally suited to function in harsh environment applications such as mission management computers, heads-up display controllers,



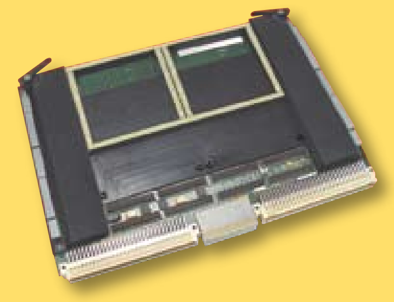
radar and sonar processors, and advanced IED automatic protection subsystems.

The C102 incorporates one or two high-performance PowerPC G4+ MPC7448 processors operating at 1.42 GHz that feature on-chip 32 Kbyte L1 and 1 Mbyte L2 caches. The board provides up to 2 Gbytes of DDR SDRAM with ECC, 256 Kbytes of NVRAM, up to 256 Mbytes of Boot Flash memory and up to 1 Gbyte of user flash memory (512 Mbytes per processor node), as well as up to 16 Gbytes of NAND onboard flash file memory for mass storage. The C102 is available in both conduction- and air-cooled models, per IEEE 1101.2 and ANSI/VITA 1-1994 specifications, respectively. Pricing for the C102 starts at $6,750.

Aitech Defense Systems
Chatsworth, CA.
(888) 248-3248.
[www.rugged.com].

PowerPC Board Sports Dual PMC Sites

Using PMC modules is one way to provide flexible expansion for VME CPUs. American ELTEC has introduced a powerful 1 GHz version of its BAB 760 PowerPC board with state-of-the-art CPU design including PCI architecture, VMEbus and expansion through



PMC modules. It offers the power of the PowerPC 750 GX CPU. The BAB 760 board can even be used for such complex tasks as image processing when combined with PMC frame grabbers. A PMC extender card permits one or two PMC modules to be fitted.

The Discovery I chip set used on the board—as well as the PCI architecture in combination with the FPGA-based VME interface—guarantees long-term availability. The BAB 760 requires only one VMEbus slot and has a double Eurocard format. A PowerPC 750 GX with a 1 Mbyte on-chip cache is used as the CPU, achieving a clock rate of up to 933 MHz; the CPU is clocked at only 933 MHz to ensure reliable operation throughout the full temperature range.

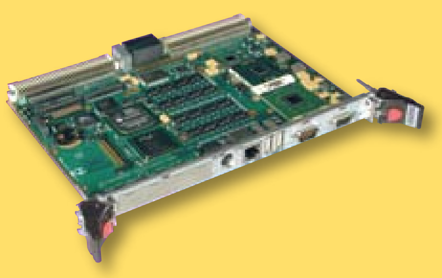
The board is equipped with an 8 Mbyte flash EPROM, providing storage for a stand-alone operating system or applications. A 512 Kbyte Boot ROM contains the initialization and test routines for start-up. Support is provided for OS-9 and VxWorks (on request) real-time operating systems, as well as ELinOS embedded LINUX. Pricing for the new 1 GHz BAB 760 Power PC board is $3,995 in single-piece quantities.

American ELTEC
Las Vegas, NV.
(702) 878-4085.
[www.americaneltec.com].

Board Combines Core Duo CPU and Optional VXS

The migration of switched fabrics into VME and the emergence of dual-core processors rank as two of the key technology trends impacting military embedded computing. Concurrent Technologies is keeping up with both those trends with its latest range of high-performance RoHS-compliant VME64x SBCs, the VX 405/04x family. The boards feature the 1.66 GHz Intel Core Duo L2400 processor and the higher performance 2.0 GHz Intel Core Duo T2500. The VXS switched serial standard VITA 41.3 is optionally supported to provide fast data transfer between other compatible boards in the system.

The VX 405/04x board supports the 2.0 GHz Intel Core Duo T2500 (in a socket) or the 1.66 GHz Intel Core Duo L2400 processor (soldered); both processors support 2 Mbytes L2 cache (shared between the cores). Up to 4 Gbytes of soldered 667 MHz DDR2 SDRAM can be installed on the boards. To enable easy fast transfer of data between the VX 405/04x board and other components in the system there are two networking options available: dual 10/100/1000 Mbit/s Ethernet interfaces (via P2) or a VITA 41.3 interface (via P0) giving dual 1000 Mbit/s baseband IEEE 802.3 serial links onto a VXS backplane fabric. A wide range of I/O is available: the front panel supports a 64-bit/66 MHz PMC (with XMC) and a third 10/100/1000 Mbit/s Ethernet interface, while both the front and rear panels support graphics,

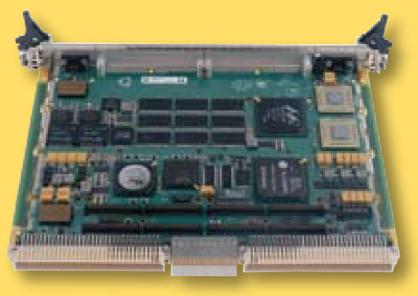


keyboard and mouse interfaces plus up to five USB 2.0 and two RS-232/422 interfaces. List prices for the 1.66 GHz Intel Core Duo L2400 processor version starts from $4,290.

Concurrent Technologies
Ann Arbor, MI.
(734) 971-6309.
[www.gocct.com].

Dual-AltiVec Board Comes in Multiple Environmental Grades

Applications such as tactical aircraft, armored vehicles and harsh environment naval systems can often share the same data and digital signal-processing needs, but each of the environmental needs of those system are dramatically different. With that in mind, Curtiss-Wright Controls Embedded Computing's SVME/DMV-183 Dual PowerPC 7447A/7448 board is available in a full range of environmental build grades.



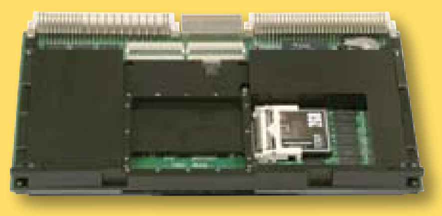
Using single or dual Freescale MPC7447A/7448 PowerPC processors with AltiVec technology and up to 2 Gbytes of state-of-the-art DDR SDRAM, the SVME/DMV-183 represents the latest advancement in functionality and performance for rugged Single Board Computers. With two 64-bit PMC sites, one supporting 100 MHz PCI-X, and an innovative complement of I/O capability such as Gbit Ethernet, up to six serial ports, up to two 1553 channels, SCSI, Serial ATA and two USB 2.0 ports, the 183 satisfies the most demanding requirements of embedded computing applications.

The processor's AltiVec-enabled e600 core (previously referred to as G4 core) delivers 9.6 Gflops peak processing power at 1.2 GHz core frequency. The board's Discovery III has a dedicated CPU-to-SDRAM path that reduces memory read latency. Up to 512 Mbytes of contiguous direct-mapped flash is provided along with 128 Kbytes of AutoStore nvSRAM with hardware write protection. The design features optimized cooling of conduction-cooled PMCs and controlled impedance routing of Pn4 I/O for digital video, StarFabric, Fibre Channel and other high-speed interfaces. Pricing starts at $9,000 for single units.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

Pentium M SBC Combines Ruggedness, Low Power

Many embedded military applications require a mix of ruggedness with low power consumption. The RPM from Dynatem, equipped with the Intel Pentium M processor, is ideal for this situation. Its high-speed 855GME and 6300ESB chipset supports a 66 MHz PCI-X expansion bus. Onboard CompactFlash permits single-slot booting. I/O routed to the backplane includes an EIDE port, two Serial ATA ports, two Gbit Ethernet ports, DVO/VGA, two USB 2.0 ports and a COM port configurable for RS-232/422/485. A PMC expansion site permits I/O tailored to users' applications. In compliance with IEEE 1101.2, the RPM comes with top and bottom cooling plates that are bonded to the major components through thermal conduction and to the heat-conducting printed circuit board mechanically. Wedgelocks secure the RPM in the chassis and bring the module's heat from the cooling plates



and the PCB to a heat plate in the chassis. The RPM has no socketed components other than the optional CompactFlash drive, so the RPM remains rugged in high shock and vibration environments.

The 855GME and 6300ESB chipset includes DRAM controller, PCI bus arbitration logic and interface, high-performance PCI, USB 2.0 interfaces, RTC, NV-RAM, standard PC timers, Ultra DMA and interrupt logic. Ultra ATA 100/66/33 IDE protocol and Serial ATA are also provided. The RPM comes populated with 512 Mbytes or 1 Gbyte of DDR-266 SDRAM with ECC and a memory bandwidth of 2.1 Gbytes/s. The 855GME offers integrated, high-performance graphics, supporting resolutions up to 1600 x 1200 at 85 MHz. Pricing for the RPM starts at $6,700 in single quantity.

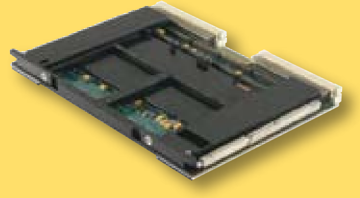
Dynatem
Mission Viejo, CA.
(949) 855-3235.
[www.dynatem.com].

Quad PowerPC Board Targets Image Processing

Advanced signal and image processing applications seem to have an ever increasing appetite for processing muscle and compute density. Feeding that need, GE Fanuc Embedded Systems today offers a multiprocessor solution called the NEXUS Quattro. This quad-processor 6U VME board is based on Freescale's MPC7447A and MPC7448 processors containing PowerPC cores. Available in versions for both rugged and benign environments, the NEXUS Quattro delivers performance and computing density typically required by radar, sonar, signals intelligence and image processing applications deployed in harsh operational environments.

The new NEXUS Quattro platform features a flexible asymmetric multiprocessing architecture that allows the four processors to operate as independent computing nodes. It can operate as a single multiprocessor or in multiple board combinations to provide an integrated, high-performance computing solution that addresses complex array processing needs in customers' systems.

Key features of the board include four Freescale Semiconductor MPC7448 processors at up to 1.4 GHz, or, four MPC7447A processors at 1.1 GHz..



Memory on board is comprised of 256 or 512 Mbytes of DDR266 SDRAM with ECC per CPU for a total of up to 2 Gbytes per board. Two PMC sites with up to 1,064 Mbyte/s peak PCI performance are provided along with ANSI/VITA 31.1 (Gbit Ethernet) support. VME320 2eSST support is implemented using the Tundra TSI148 PCI-X-to-VME Bridge for up to 320 Mbyte/s VME performance and compatibility with legacy VME designs.

GE Fanuc Embedded Systems
Huntsville, AL.
(256) 880-0444.
[www.gefanuc.com/embedded].

VXS SBC Functions as Two Boards in One Slot

Redundant computing nodes are vital for many mission-critical defense applications. That used to mean two or more separate boards, taking up extra backplane slots. General Micro Systems offers a way to do that using just a single board. A VXS 4.3-based processor board, the new V469 Patriot replaces anywhere from two to four VME boards. This 6U board is a true dual-processor architecture, with each processor sharing absolutely nothing with the other processor, as if they were in two different VME slots.

The two processors are linked together with the Gigabit Ethernet or may be linked via VITA 41.3 VXS, thus providing a massive server density unlike any other technology. To provide even more processing muscle at lower power, the new dual core processors will be used to provide quad-processing capabilities. The V469 utilizes two of the new M-760 Pentium M processors, each operating at 2.0 GHz with 2 Mbytes of L2 Cache and 533 MHz FSB. The V469 provides up to 8 Gbytes of 266 MHz RDDR memory with ECC. Standard I/O functions on each side of the Patriot include: dual Gigabit Ethernet ports with Copper or Fibre interface, 2 Gbit, full duplex Fibre Channel with 2 Mbytes of SRAM buffer and Flash

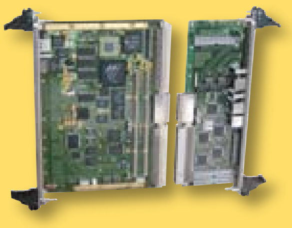
BIOS to support Boot capabilities, quad USB 2.0, dual Serial ports, XVGA Video andUDMA IDE interface. An optional I/O interface module allows one Compact Flash and one USB 2.0 device to be added to each side. Pricing for the 4 Gbyte V469 Patriot starts at $4,700 (100s).

General Micro Systems
Rancho Cucamonga, CA.
(909) 980-4863.
[www.gms4sbc.com].

VME64x/2eSST SBC Serves Up 1.7 GHz PowerPC

VME and the PowerPC processor architecture together form the heart of today's installed base of military embedded computer systems. Supporting that tradition, Interface Concept has rolled out a new VME SBC based around the Freescale 1.7 GHz MPC7448 PowerPC. This low-power PowerPC design provides 1 Gbyte of SDRAM-DDR with ECC. Both fast NOR and large NAND flash memories are implemented on board.

The IC-e6-VMEa runs as a system controller or a standard single-slot board. An automatic detection can be used with the VME64x backplane. The VMEbus interface is based on a combination of the Tundra Tsi148 VME bridge and the latest generation of Texas Instruments transceivers. The 2eSST bus protocol



capabilities provide up to 300 Mbyte/s transfer rates across the VMEbus. The board supports three Gbit Ethernet channels, one console port and one USB 2.0 controller. A quad UART provides four additional asynchronous channels available on the P2 connector. The 64-bit PCI/PCI-X bridge allows the VME SBC to control two PMC mezzanine boards with the PnIO routed according to the VITA 35. Thanks to its SATA controller, the IC-e6-VMEa can manage directly four storage devices. The IC-e6-VMEa board can operate from -40° to 75°C. The conduction-cooled version runs at 1.4 GHz. Prices start at $4,800.

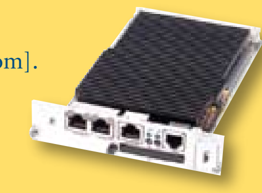
Interface Concept
Briec de l'Odet, France.
+33 (0)2 98 57 30 30.
[www.interfaceconcept.com].

660 MHz PowerQUICC III Rides 3U VME

The 3U flavor of VME offers a compact solution for space-constrained military applications. And with today's level of integration, the same functionality that used to require one or more 6U cards can be offered in a 3U solution. Along those lines, the VMP3 from Kontron Modular Computers sports a Freescale PowerQUICC III RISC processor, MPC8541. This PowerPC board, with a maximum clock-rate of 660 MHz, offers two integrated Gigabit Ethernet ports. The challenges of network bandwidth and security are met by the Hardware Security Engine, which is integrated into the processor and supports encryption in accordance with IPSec, DES, 3Des and AES. These features, along with the very fast DDR SDRAM, make the VMP3 a universal processor card for computing-intensive real-time military applications.

The 100 x 160 mm board has up to 256 Mbytes of directly soldered DDR SDRAM, 16 Mbytes of flash, 1 Mbyte of buffered SRAM and E²Prom for user and configuration data. A slot for CompactFlash memory cards is optional. A Fast Ethernet interface and a serial port supplement two Gigabit Ethernet ports. Additional features are: watchdog, real-time clock and a temperature sensor. The VMP3 is designed for temperature ranges from 0° to 60°C and is optionally available for -40° to +85°C. Pricing for the VMP3 starts at $1,295 in OEM quantities. Single piece pricing starts at $1,995.

Kontron America
Poway, CA.
(858) 677-0877.
[www.kontron.com].



Dual 1.4 GHz PowerPC Card Supports RapidIO or PCIe

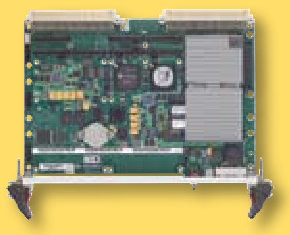
Among the great successes of the VME community was its diligence in marrying switched fabric technologies with embedded form-factors. That process started long before the military had any interest in switched fabrics. And now that they do, products like Mercury's Momentum Series VPA-200 Dual 7448 VXS SBC is ready to fill that role. The board is a full-featured 6U VME board that offers a higher level of computing power and bandwidth for users with high-density needs. The dual Freescale 1.4 GHz MPC7448 PowerPC processors are combined with high-bandwidth VITA 41 functionality and a range of versatile I/O options to deliver performance and flexibility to system designers. The board uses a Marvell GT64460 bridge with a 167 MHz MPXbus. DDR-400 SDRAM, with optional ECC, is provided up to 1 Gbyte.

The VPA-200 was the industry's first VME host board to support dual PowerPC 7448 processors and the RapidIO fabric (VITA 41.2), or a PCI Express interconnect (VITA 41.4) on the VXS multi-gigabit P0 backplane fabric connector. VME P0 has dual Gigabit Ethernet ports for command/control or I/O interconnect. A Tundra Tsi148 VME bridge chip provides VME 2eSST support and two PMC sites. Each PMC site is connected to both a processor node and the fabric bridge/switch. And each PMC is also user-configurable for 100 MHz PCI/X or 66 MHz PCI. The card supports Linux or VxWorks operating systems, and is available now for $7,000 in OEM quantities.

Mercury Computer Systems
Chelmsford, MA.
(978) 256-1300.
[www.mc.com].

Freescale 8540 Board Is Low-Power VME Solution

VME users are often looking for faster, more powerful processors to upgrade their systems or implement new ones while retaining their software investments. For them, Motorola offers a VME upgrade or growth path with the MVME3100 family of SBCs featuring the system-on-chip MPC8540 from Freescale. This SoC implementation provides power/thermal, reliability and life cycle advantages not typically found in other architectures. The MPC8540 comes with a PowerPC processor core, integrated memory controller, PCI-X interface and 667 MHz and 833 MHz options. Now, customers can keep their VMEbus infrastructure—chassis, backplanes and other VMEbus and PMC boards—while improving the performance and extending the life cycle of their systems.



Two versions of the MVME3100 are offered. The MVME3100-152 provides a 667 MHz processor, 256 Mbytes of DDR ECC SDRAM and 64 Mbytes of flash. The MVME3100-1263 has an 833 MHz processor, 512 Mbytes of DDR ECC SDRAM, 128 Mbytes of flash and a PCI expansion connector. Both boards provide Gigabit Ethernet ports for connection to enterprise and real-time networks, serial ports, USB 2.0 and SATA controllers. A Tundra Tsi148 PCI-X to VMEbus bridge supports the VME64 and 2eSST protocols. For expansion, these Motorola boards also have dual PMC-X sites with front panel access supporting PCI-X bus speeds of 33, 66 or 100 MHz. An optional MVME721 rear transition module (RTM) allows I/O routing through the back of the VMEbus chassis. Board support packages for VxWorks and Linux are available. Pricing ranges from $1,800 to $2,400, depending on options.

Motorola
Tempe, AZ.
(602) 538-5720.
[www.motorola.com/computing].

Board Blends Dual PowerPCs and Switched Fabrics

In complex multiprocessing systems, it's not enough to just have power processing muscle. Equally important is an ability to move data between processors and boards to keep those processors fed. Responding to such needs, Radstone Embedded Computing offers the XtraPower PPCM2 6U VME Dual PowerPC Processor. Featuring two fully independent PowerPC 7448-based compute nodes, the PPCM2 also provides two StarFabric ports as well as two Gigabit Ethernet ports and four serial ports.

The loosely coupled architecture of the PPCM2—in which each processor has its own memory resources—means that it is uniquely suited to the support of real-time operating systems and real-time applications, running separate instances of the chosen operating system per node. Supported operating systems include VxWorks from Wind River, LynxOS from LynuxWorks and INTEGRITY from Green Hills Software. Mission-critical applications also benefit from Radstone's comprehensive Deployed Test software for the PPCM2.

Each node has its own dedicated I/O resources including GPIO, serial and Gigabit Ethernet, and achieves superior I/O management by dedicating one PCI-X-capable PMC to each processor. Shared resources include further GPIO and USB 2.0 plus 2eSST VME and two StarFabric ports. The

PPCM2 features Marvell's latest Discovery III Integrated System Controller supporting high-capacity DDRAM, flash memory and NVRAM. The PPCM2 can be ordered in any one of five ruggedization levels. Pricing is from $8,550.

Radstone Embedded Computing
Billerica, MA.
(800) 368-2738.
[www.radstone.com].

VME Blade Sports Dual-Core Xeon CPU

The trend toward multicore processors is sweeping across the computing world, and the embedded computing market is riding that wave. The military's desire to pack in as much compute density as possible couldn't be happier with this technology direction. Thales Computers latest dual-core board is its PENTXM2, a server class manageable VMEbus blade based on the low-power Intel dual-core Xeon processor. The PENTXM2 uses the 1.67 GHz dual-core Xeon, combined with the Intel E7520 server class memory controller hub (MCH).

The board is available with up to 4 Gbytes of DDR2-400 SDRAM. When paired with the support of VITA 31.1 backplane networking, the PENTXM2's VITA 38 intelligent platform management interface (IPMI) feature provides for easy scaling into a multiprocessing system. The PENTXM2 runs Red Hat Linux and features as an extensible firmware interface (EFI) standard BIOS/Firmware that is able to boot Linux 2.6, VxWorks, Lynx OS, Microsoft Windows and Red Hat Linux operating systems. The PENTXM2 is available as a stand-alone board component or pre-integrated in large systems (PowerMP6) with full data transport and management software based on standards such as MPI and HTTP.

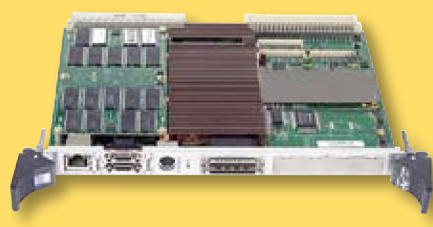
The PENTXM2 provides a dual SATA-150, a triple USB 2.0 port and an EIDE interface for an onboard disk or compact-flash support. Pricing for the PENTXM2 starts at $3,950 in small volume and subject to specifications. A rugged conduction-cooled version of the PENTXM2 will be available in the third quarter of 2006.

Thales Computers
Raleigh, NC.
(919) 231-8000.
[www.thalescomputers.com].

Turion64-Based SBC is Upgrade Path for Sparc Boards

AMD has been a leader in 64-bit processor offerings. In the VME space, the AMD's Turion 64 Mobile processor serves as a natural upgrade path for legacy Sparc-based Solaris designs. Serving that need, Themis Computer offers its TA64 board, the first in a series of 6U VMEbus computer boards and is based on AMD's Turion 64 Mobile processor. The TA64 is backward compatible with Themis' USPIIe SBC, at the application source code level, and features front panel and backplane compatibility, including all I/O, switches and indicators. The TA64 runs 32-bit Sun/Solaris 8 and 9, and 64-bit Solaris 10, Windows and Linux.

The TA64 has an onboard PMC Slot and inter-board stacking connector that allows expansion for graphics and PMC carrier cards. It includes a high-performance Universe II VME64x interface, dual Ultra320 interface, two 10/100/1000 Ethernet ports, two or more USB



ports, AC97 audio, two serial ports and one PS/2 port. These VME64 boards are available in one, two and three slot configurations that offer a wide range of I/O and performance options. The TA64 single-slot configuration features a single Gigabit Ethernet port, support for Dual Ultra320 SCSI drives and a single 64-bit PMC slot. Memory is expandable to 4 Gbytes of DDR333 memory. The board has 45W power dissipation, which is low for a board of its class. OEM pricing for the board is below $5,000.

Themis Computer
Fremont, CA.
(510) 252-0870.
[www.themis.com].

COTS Products

Tiny Board Networks Controllers and Operator Interfaces

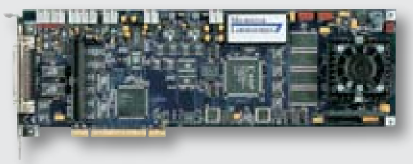
Embedded networking is poised to make a big splash in military system designs. The vision is for every component on an aircraft wing to have its own IP address holding status information that can be accessed from anywhere on the DoD's network. Mosaic Industries has released its Ethersmart Wildcard, a 2 x 2.5-inch expansion board that brings Web connectivity to any of Mosaic's embedded controllers and operator interfaces.

This low-cost peripheral card connects with standard Ethernet cables, allowing instruments to communicate with other computers on a Local Area Network (LAN). With it, you can connect to your controller from a Web browser to monitor its status, diagnose problems or update its software. An application program can send emails to transmit data or alert other computers on the network when significant events occur. This new member of Mosaic's Wildcard family uses the Lantronix XPort, which combines an x86 processor, flash memory, 10/100 Mbit Ethernet network interface controller and RJ45 jack. An onboard UART (Universal Asynchronous Receiver/Transmitter) buffers data between XPort and host controller. The XPort can be shut down while the interface is not in use to conserve power. The Ethersmart Wildcard is available immediately and is priced at $140 in 100s.

Mosaic Industries, Newark, CA. (510) 790-1255. [www.mosaic-industries.com].

Board Pentium Processing with Real-Time Data Acq

When real-time processing is done right on a data acquisition board it frees the host processor from system delays. Along just such lines, MicroStar offers its DAP 5000a/526, powered by an Intel Pentium 233 MHz CPU. The card includes 16 analog inputs, 2 analog outputs, 16 digital inputs and 16 digital outputs. External rack-mounted hardware can extend these channel counts to 512, 66, 128 and 1024 respectively. The board can acquire 14-bit data at up to 800 ksamples/s, and can convert 833 kvalues per second on each of the two onboard analog outputs. The onboard Pentium processor allows fast real-time processing, and low latency—0.1 ms task time quantum—provides for fast response.

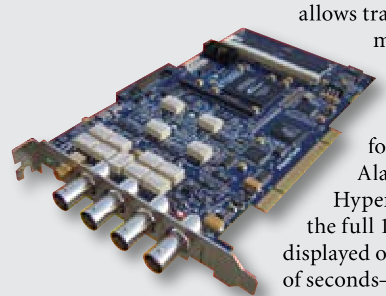


A DAP board provides an additional processor running a real-time operating system, DAPL, that can be controlled from a Windows application. This provides an extra resource and lets you apply computing power when and where needed. DAP boards acquire data, converting analog signals into digital values. The onboard processor performs any required operations as it transfers data from pipe to pipe. The new mid-range DAP 5000a/526 board includes an Intel Pentium 233 MHz CPU. The DAP 5000a/526 costs $3,195. DAPstudio costs $199.

Microstar Laboratoires, Bellevue, WA. (425) 453-2345. [www.mstarlabs.com].

16-bit PCI Digitizer Boasts 125 Msample/s Rates

Gone are the days when high-speed analog to digital conversion required large costly racks of instrumentation. Now fast digitization for RF signal analysis, radar and lidar can be done with a low-cost PCI card. With that in mind, AlazarTech announced the release of ATS660, a 16-bit PCI waveform digitizer with two simultaneous analog inputs that can each be sampled at rates up to 125 Msamples/s, providing a Signal to Noise Ratio in excess of 73 dB. Each channel can have up to 128 Msamples of onboard acquisition memory buffer. The unit occupies only one half-length PCI slot. ATS660 features Dual Port Acquisition Memory that allows transfer of acquired data to PC memory without having to stop the acquisition session.



ATS660 PCI digitizers use FPGA-based digital electronics for control and data processing. AlazarTech's proprietary HyperDisP display technology allows the full 128 Msamples-long record to be displayed on a computer screen in a matter of seconds—an improvement of many orders of magnitude compared to the competition. Available in mid-September, pricing for the ATS660 ranges from $4,495 to $5,495 depending on configuration.

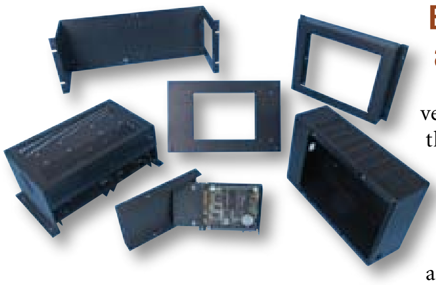
AlazarTech, Montreal, QC, Canada. (514) 633-0001. [www.alazartech.com].

200W DC-to-DC Converter Aims at Tactical Military Apps

Power considerations are often done at the back end of many system designs. Fortunately there's a wealth of military power solutions available to solve those afterthought situations. Rantec's HDM-200 is a line of single output DC-to-DC converters for the military's most demanding systems applications and environments. The DC-to-DC converter line operates from standard military (MIL-STD-704) 270 VDC and provides isolated output voltages ranging from 1.5 VDC to 28 VDC. Through the use of fixed frequency, secondary side control, the modules have superior noise immunity and rejection and dynamic line and load response.

Originally designed for the JSF program, the module uses mu-metal shielding for ultra low radiated emissions. The module is 2.3 x 2.4 x 0.5 inches, weighs less than 3.1 oz and operates from -55° to +85°C. The feature-rich module has remote sense, active parallel capability, remote shut down, synchronization and input and output voltage trim. In addition, it has status signals for over-current, over-voltage, output good and temperature. This all equates to a DC-to-DC converter that is easy to integrate in tactical military applications and provides the intelligence and flexibility required for today's systems. The HDM-200 is priced at $310, quantity 100.

Rantec Power Systems, Los Osos, CA. (805) 596-6000. [www.rantec.com].



Enclosure Family Targets EPIC, EBC and PC/104

The rigid separation between board vendor, system vendor and enclosure vendor has begun to blur over the past couple years, as board vendors expand their offerings to include enclosure solutions. Following just that trend, Micro/sys offers a variety of enclosures with mounting holes for PC/104, 5 x 5-inch EPIC and/or EBX-sized computer boards, and can hold up to three stacked PC/104 modules. To maximize options and make field service or maintenance easier, the enclosures are designed with multiple cable and connector cutouts and terminal block/accessory mounting holes.

Micro/sys enclosures range from a 19-inch rackmount frame that is 3U high to a small unit that houses microcontrollers or a single PC/104 board. There are LCD Flat Panel Enclosures in 6.4, 10.4 and 17-inch sizes for systems that require the embedded computer box to be separate from the display. These flat panel enclosures are louvered for airflow and heat dissipation. When a box solution is needed, there are two Embedded Computer Enclosure versions, one with terminal blocks mounting externally, and one with a 6.4-inch LCD Flat Panel Display. The Micro/sys enclosures start at $75 in single quantities while significant OEM discounts are available.

Micro/sys, Montrose, CA. (818) 244-4246. [www.embeddedsys.com].

SCSI Flash Disk VME Module Ready for Rough Duty

These days, even the most harsh environment military systems are demanding generous amounts of fast data storage. Phoenix International Systems has introduced the first solid-state disk plug-in VME module with 320 Mbyte/s speed, its new single-slot module VL1-350-SC-SSD. The new Ultra 320 SCSI Solid State Flash Disk Module is the only VME storage product on the market that combines the ability to perform in challenging environments, where high altitude, extreme temperatures, shock, vibration, rapid changes in air pressure (explosive decompression) and electromagnetic radiation are factors, all with 320 Mbyte/s speed.

The VL1-350-SC-SSD model is backward compatible with existing systems including SCSI-2 and SCSI-3 interfaces. Due to its unique design, it eliminates seek time, latency and other electromechanical delays inherent in conventional disk drives. The product also features 320 Mbyte/s burst R/W rate, 50 Mbyte/s sustained read and sustained writes rates. The device offers an unformatted storage capacity to 128 Gbytes and access times of less than 0.02 ms. The unit operates at altitudes to 80,000 feet and meets shock, operating and non-operating specs at half sine, 1500G, 0.5 ms per MIL-STD-810F. Operating temperatures from -40° to + 85°C are supported. List price ranges from $2,445 for the 8 Gbyte VL1-350-SC-SSD-8 to $17,147 for the 128 Gbyte VL1-350-SC-SSD-128, with quantity discounts available.

Phoenix International, Orange, CA. (800) 203-4800. [www.phenxint.com].

USB Data Acq System Accepts Eight Sensor Inputs

Vibration testing ranks as one of the most critical areas of military system development. Thanks to the magic of system integration, data acquisition systems for vibration analysis are available in compact USB-based systems rather than bulky rack and chassis level systems. Exemplifying that trend is Data Translation's new DT9841-VIB, a real-time DSP data acquisition Sleek Box capable of accepting eight simultaneous IEPE sensor inputs. The DT9841-VIB is the latest addition to the Fulcrum II Series of DSP data acquisition products for USB 2.0. The DT9841-VIB provides excitation, signal conditioning and anti-aliasing filtering for real-time high-accuracy IEPE sensor values.

The DT9841-VIB board contains eight, simultaneous 24-bit sigma-delta analog input channels with a sampling rate of 100 kHz per channel. In addition, the board has two 24-bit deglitched waveform analog output channels to control a shaker table for example, and stimulate systems under test, 16 digital I/O lines for control and monitoring, and three 32-bit counter/timers providing highly accurate timing functions. All subsystems can be run simultaneously and monitored in real time with an onboard 32-bit floating-point processor. The board offers sampling rates up to 100 kHz per channel and uninterrupted data transfer. The DT9841-VIB, available in a Sleek Box version, is priced at $5,690.

Data Translation, Marlboro, MA.
(508) 481-3700. [www.datatranslation.com].

EBX Development Kit Targets Linux Designs

Linux has become a popular development platform for a number of military programs. Software engineers enjoy a familiarity with it, and it's free of the costs and complications of dealing with a traditional embedded OS. Serving that need, Arcom's new Development Kit allows faster and easier development of embedded systems in a Linux environment. The kit's SBC-GX533 board has a compact Arcom Embedded Linux image installed in its onboard flash.

The kit's SBC-GX533 board is well suited for deeply embedded, remote or unattended installations demanding reasonable processing power. It is a low-profile, fan-less, RoHS-compliant EBX form-factor board, based on a 400 MHz AMD Geode GX533 1.1W processor. It has 512 Mbytes of DDR DRAM and 32 Mbytes of flash installed, of which 13 Mbytes are used by the Linux image. The board also features TFT or CRT support, an analog touchscreen interface, dual 10/100BaseT Ethernet ports, CompactFlash (CF+), 4 serial and 4 USB ports. Industrial expansion is provided through an 8-bit TTL I/O port, a PC/104 and a PC/104+ site. All usual PC interfaces are also included. Pricing for this development kit is from $997.

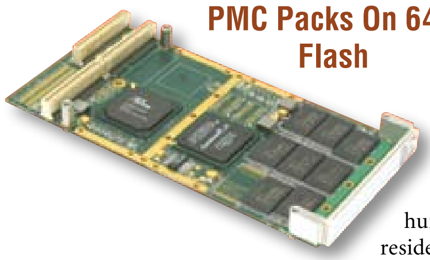
Arcom, Overland Park, KS. (913) 549-1000. [www.arcom.com].

Chassis Brings Liquid Cooling to Rugged Apps

Faster, denser computing is in high demand, but that means more heat. Liquid-cooling solutions are emerging that are uniquely packaged for high-speed airborne or ground-based signal processing applications such as radar, SIGINT and electronics warfare. An example is Parker Hannifin's liquid flow-through (LFT) electronics chassis. The packaging for the LFT demonstrator chassis is an air transport rack (1-ATR long) standard-sized enclosure of approximately 8"h x 10"w x 20"l. The system is entirely self-contained, with its own closed-loop liquid-cooling system. The system contains coolant, a control system, smart pump, filter, accumulator, heaters (for cold-system start-up), and three different board-level heat-absorbing technologies to demonstrate the variety of options available to the electronics designer.

Parker's LFT chassis is capable of cooling up to a maximum of 850 watts per slot, a total of 2,000 watts with dielectric fluids such as hydrofluoroethers (HFE) and synthetic oil (PAO), or 4,000 watts with non-dielectric fluids such as water or water/glycol mixtures. The product can be scaled to accommodate the required amount of technology integration for individual applications, and is hybrid-backplane-capable to accommodate any board technology, including VME, VITA 41/VXS and VITA 46-48/VPX (REDI). Pricing for the LFT electronics chassis ranges from $25,000 to $35,000, depending on options and volume.

Parker Hannifin, Mentor, OH. (440) 954-8100. [www.parker.com/advancedcooling].



PMC Packs On 64 Gbytes of NAND Flash

The net-centric vision for the military calls for lots of sharing of detailed map, sonar and radar data, and those memory-hungry applications must reside in rugged embedded applications. Feeding that need, Aitech Defense Systems now offers a high-density PMC that provides up to 64 Gbytes of NAND Flash memory in two banks. The new M222 provides a sustained data transfer rate of up to 40 Mbytes per second and low power consumption of less than 7W. Designed for high-speed read, write and erase performance, the M222 is suitable for high-density, local data storage applications such as detailed maps, large databases, radar or sonar images, software programmable radio ELINT data or other graphics.

Available in commercial, rugged and military grade configurations, the M222 Flash memory PMCs are designed to resist shock and vibration for trouble-free performance, even in high-stress military environments. The M222 is available in forced air-cooled and standard ANSI/VITA 20 conduction-cooled mechanical formats. Both versions are single-slot PMC modules that connect and take all of their power from the CompactPCI, VMEbus or PCI base board. Pricing for an 8 Gbyte M222 starts at $5,670.

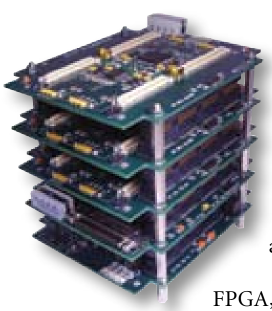
Aitech Defense Systems, Chatsworth, CA. (888) 248-3248. [www.rugged.com].

3.5-in. SBC Is Upgrade Path for Geode GX1 Systems

For small, mobile military systems like battlefield robots and UAVs, there's nothing more critical then the blending of low power with hefty processing muscle. Feeding that need, Advantech's PCM-9375 is its newest 3.5-inch biscuit SBC with the richest set of embedded features. With a AMD Geode LX 800@0.9W processor onboard, the PCM-9375 has the same mechanical design and layout as its predecessor, and offers an ideal upgrade path for older AMD Geode GX1processor-based systems.

PCM-9375's rich array of features includes up to 512 Mbyte DDR SODIMM memory, 4 COMs (1 x COM port supports RS-422/485), 4 x USB 2.0, 1 Enhanced IDE interface, AC97 audio, 8-bit GPIO (general-purpose input/output),1 CompactFlash type II slot, 2 Fast Ethernet and one PC/104 slot. Amazingly, PCM-9375's total power consumption is around 6W with 256 Mbytes of DDR memory and 256 Mbyte CompactFlash. PCM-9375 was specially developed with Windows Embedded OS optimized drivers, tools and components to enhance Microsoft Windows CE 5.0 and XPe (SP2). With the Advantech OS image, you get additional useful features, like Auto Launch Application, Registry Editor, Registry Flusher and AdvLib (SMBus, WatchDog, I2C and GPIO), helping customers develop richer and more dynamic CE-based applications. Price is $280 per unit.

Advantech, Irvine, CA. (949) 789-7178. [www.advantech.com].



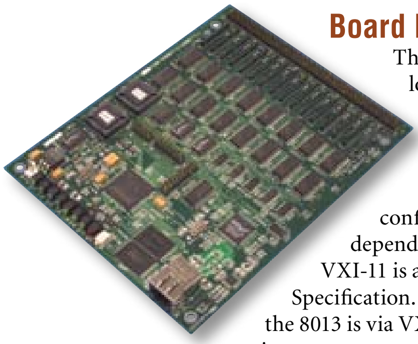
FPGA-Based PC/104 Processor Card Provides Development, Deployment Options

High-performance signal processing systems, like those used in SIGINT and software radio, increasingly depend on FPGAs to handle specialized processing functions. A new PC/104 card stack from Nallatech takes advantage of multiple FPGAs to handle processing and system management, while providing expansion slots for additional system resources.

The BenNUEY-PCI-104-V4 can support multiple analog and digital I/O interfaces and multiple memory types, as well as up to seven FPGAs, in a single PC/104 stack. Three DIME-II expansion slots let engineers optimize system resources to meet processing, memory and I/O requirements. The BenNUEY-PCI-104-V4 comes with an onboard Xilinx Virtex-4 FPGA. Up to six additional FPGAs are available on the DIME-II expansion modules, which support Virtex-4, Virtex-II Pro and Virtex-II FPGAs.

Applications requiring data storage will benefit from the 16 Mbytes of DDR-2 SRAM connected to the Virtex-4 FX user FPGA, which can be used for storing algorithmic data or for buffering data around the multi-FPGA architecture. An Ultra-SCSI connector provides digital I/O. Linux and Windows are supported, and FUSE FPGA Computing Runtime Software is included. Pricing for the BenNUEY-PCI-104-V4 starts at $19,995.

Nallatech, Glasgow, Scotland. +44 (0) 1236 789518. [www.nallatech.com].



Board Links Ethernet to Digital I/O

The military has warmed to Ethernet in a big way. It offers just the right kind of ubiquity and longevity that long life cycle programs need. ICS Electronics has put Ethernet to work for digital I/O duty with a new Ethernet to Digital Interface Board for controlling digital devices. Called the Model 8013, this new Interface Board provides 128 digital I/O lines that the user can control from any computer with a NIC interface or from a TCP/IP network.

The Model 8013 is an Ethernet to Parallel Interface that provides 128 parallel I/O lines that can be configured as inputs or outputs in 8-bit bytes. Data transfer can be done by a combination of three methods depending upon the needs of the devices connected to the 8013. The Model 8013 is a VXI-11.3-compliant Interface. VXI-11 is a communication standard developed by the VISA consortium in 1995 in conjunction with the VISA Specification. VXI-11.3 is a sub-standard that covers TCP/IP-to-Instrument servers like the 8013. Communication with the 8013 is via VXI-11 RPC protocol over a TCP/IP network. Pricing for the Model 8013 is $495 each in quantities of 1 to 4 units.

ICS Electronics, Pleasanton, CA. (925) 416-1000. [www.icselect.com].

Dual-Core Xeon VME Blade Aims at Naval, Aerospace Apps

The latest generation of naval and airborne graphics subsystems has significantly improved graphics performance, such as multi-head display and high-resolution video grabbing. Supporting this trend, Thales Computers has introduced the first server-class manageable VME blade based on Intel's dual-core Xeon processor.

The PENTXM2 uses the 1.67 GHz dual-core Xeon combined with the Intel E7520 server class memory controller hub. Up to 4 Gbytes of DDR2-400 SDRAM is provided, along with a dual SATA-150, a triple USB 2.0 port and an EIDE interface. The board's VITA 38 intelligent platform management interface (IPMI) feature provides easy scaling into a multiprocessing system when combined with the support of VITA 31.1 backplane networking.

The PENTXM2 runs Red Hat Linux and features as an extensible firmware interface (EFI) standard BIOS/firmware that can boot Linux 2.6, VxWorks, Lynx OS, Microsoft Windows and Red Hat Linux. It is available either as a stand-alone board or pre-integrated into large systems (PowerMP6) with full data transport and management software based on standards such as MPI and HTTP. Pricing starts at $3,950 in small volumes.

Thales Computers, Raleigh, NC. (919) 231-8000. [www.thalescomputers.com].

Multi-Processor VME Board Provides High Throughput, Low Latency

A new multi-processor VME board from Cornet Technology provides the high throughput and low latency needed to support a wide variety of intricate military/aerospace applications that require multi-processing power.

The Celero CVME-7410 features up to four independent PowerPC nodes linked by a PCI bus on a single VME board to help designers handle complicated processing functions, such as image processing, digital signal processing, sonar control and radar control. The board supports LINUX and is the first VME board to support the VxWorks Safety Critical platform. This enables system designers to develop systems that are compliant with ARINC-653 and DO-178B, which are recommended and often mandated by military and avionics programs.

The Celero VME-7410 will be available for shipping in the third quarter of this year. Pricing starts at $14,995.

Cornet Technology, Springfield, VA. (703) 658-93400. [www.cornet.com].

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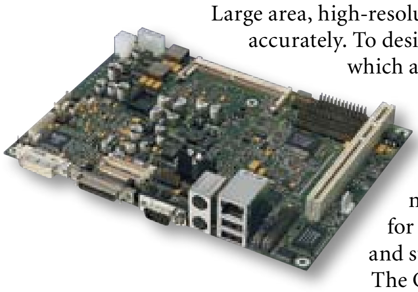
SBC Controls Large Area, High-Resolution LCD Displays



Large area, high-resolution TFT LCDs are used in a growing number and variety of military applications to display data accurately. To design the subsystems that control these displays, defense engineers need the right combination of features, which are provided by a new EBX form-factor SBC from Apollo Display Technologies.

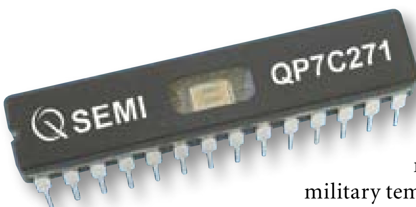
The Galaxy SBC features either the 400 MHz or 650 MHz Intel ULV Celeron processor and up to 512 Mbytes of SO-DIMM in a compact, 8-in. x 5.75-in. form-factor. The fanless design minimizes power loss and heat buildup. Four versions are available: a Best Performance version with an Intel 815 chipset for simple 2D, two High Performance versions with M6 or M7 ATI graphics and 16 Mbytes of graphics memory, and a High-End Performance version with M9 ATI graphics and 64 Mbytes of graphics memory for high-end 3D. This version includes driver support for dual display mode, with separate content per display, and supports portrait/landscape display modes.

The Galaxy supports popular operating systems such as Microsoft Windows, Win CE and Linux. Delivery is typically 6-8 weeks. Pricing for the Best Performance version is $232.07 in production quantities of 10K units.

Apollo Display Technologies, Ronkonkoma, NY. (631) 580-4360. [www.apollodisplays.com].

High-Speed CMOS UV PROMs Sport Hermetic Packages

A family of CMOS UV PROMs that feature low power consumption and speeds down to 15 ns are complete redesigns of widely used Cypress Semiconductor parts. The pin-for-pin replacements from QP Semiconductor are available in hermetic packages for military and aerospace applications.



The family of 8-bit-wide memories covers the full military temperature range and offers proven high programming yield. The PROMs are available either as one-time-programmable (OTP) devices or in windowed packages and feature TTL-compatible I/Os. Memory cells utilize proven CMOS PROM floating-gate technology. The PROMs are available in sizes ranging from 4K to 512K.

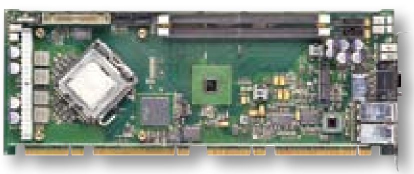
The devices are available in either industrial-grade hermetic packages or fully mil-qualified QML hermetic packages. Windowed and windowless package types include standard 300- and 600-mil DIPs, flatpacks and leadless chip carriers. Pricing in quantities of 100 pieces begin at $12.50 each depending on package type and screening requirements.

QP Semiconductor, Santa Clara, CA. (408) 737-0992. [www.qpsemi.com].

Graphics-Class System Host Board Provides 20 PCI Express Lanes

PCI Express may not have been the first switched fabric to be adopted by military system designers, but it will be the most widely used. A new system host board (SHB) from One Stop Systems is a graphics-class, PICMG 1.3-compatible board that offers 20 lanes of PCI Express (PCIe).

The MaxExpress Pentium D system host board supports x16, x4 and x1 PCIe links, as well as a 32-bit/33 MHz PCI interface. It easily accommodates a wide range of system option cards, from the latest x16 PCIe video cards to legacy 32-bit/33 MHz PCI cards. Socket-LGA775 processor options support 32-bit and 64-bit applications and have larger L2 cache memories. The Intel 945G MCH and ICH7R ICH chipset delivers advanced dual-core SHB capabilities to easily handle the most demanding applications.

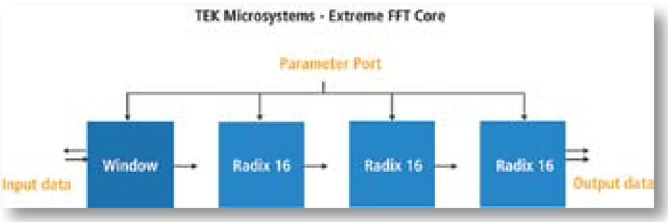


The board's dual-core design supports dual 10/100/1000Base-T Ethernet interfaces, while primary and secondary SATA/300 ports support up to four independent SATA storage devices. The SATA controller can be configured as a RAID controller supporting RAID 0, 1, 5 and 10 implementations. The SHB lists for $2,861 without DRAM.

One Stop Systems, Escondido, CA. (760) 745-9883. [www.onestopsystems.com].

FPGA FFT Core Is 10x Faster

A new FPGA FFT core for signal processing applications performs 4K point FFTs at least 10 times faster and more efficiently than any previous implementation. It is targeted at demanding military and industrial signal processing applications and can significantly reduce system size, weight and power.



The Extreme FFT Core from TEK Microsystems performs up to one million 4K point FFTs/s, and is pre-integrated with TEK Microsystems' Neptune and Triton VXS-based products. It features run-time programmable FFT sizes of 1, 2 and 4K along with a run-time programmable window. This design uses only about 10K slices, which takes up about one-third of a Xilinx Virtex II Pro 70, and incorporates optimized arithmetic for maximum signal/noise ratio.

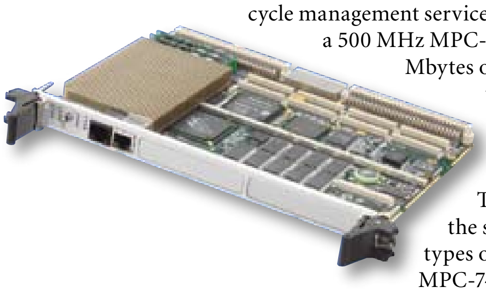
Pricing of the Extreme FFT Core is $10,000.

TEK Microsystems, Chelmsford, MA. (978) 244-9200. [www.tekmicro.com].

SBCs Offer Alternative to Legacy Motorola Boards

Long-term availability and life cycle management support are two major needs of military system designers. Three new single- or dual-processor SBCs from Curtiss-Wright Controls Embedded Computing provide slot-replacement alternatives to the legacy Motorola single-processor MVME5100, MVME5500 and MVME6100.

The Falcon/51x, Raptor/55x and Manta/61x VMEbus SBCs offer functional compatibility and competitive performance, as well as life cycle management services. The Falcon/51x has a 500 MHz MPC-7410 processor with 2 Mbytes of L2 cache per CPU, up to 1 Gbyte of 133 MHz DRAM and 128 Mbytes of NOR flash with Altboot. The Raptor/55x has the same amount and types of memory, a 1+ GHz MPC-7457 and a 512 Mbyte NAND Flash File System. The Manta/61x has the same processor, L3 cache and NOR flash as the Raptor, but with up to 2 Gbytes of 133 MHz DRAM and a 1 Gbyte NAND Flash File System. Various combinations of I/O, including PMC sites, Ethernet, FireWire, COM and SATA are provided for each version.



The SBCs are designed for commercial and semi-rugged military application environments. For more demanding applications, each is available in extended ruggedization levels, including conduction-cooled versions. Support for OS environments such as Linux and VxWorks is provided. In quantity volumes, pricing starts at under $3,000.

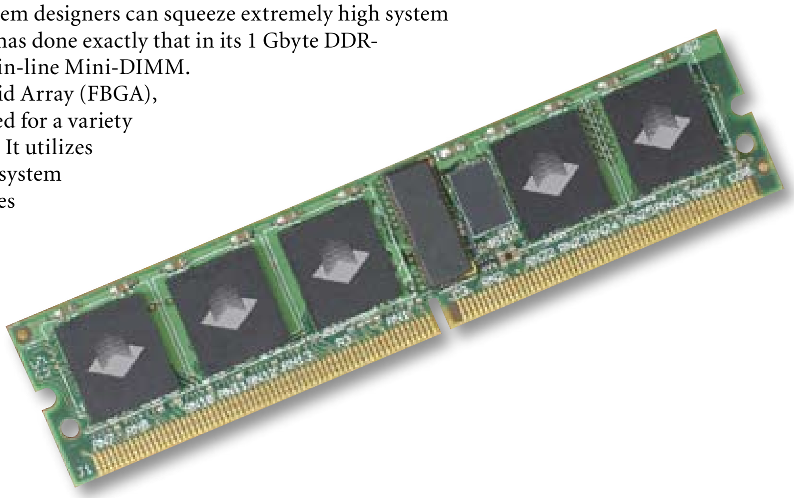
Curtiss-Wright Controls Embedded Computing, Dayton, OH. (937) 252-5601. [www.cwcembedded.com].

Mini Module Packs In 1 Gbyte of DDR-2 SDRAM

By packing multiple DRAM die onto a mini module, military system designers can squeeze extremely high system densities into a compact reliable package. White Electronic Designs has done exactly that in its 1 Gbyte DDR-2 SDRAM Fine Ball Grid Array (FBGA) very low profile (VLP) dual in-line Mini-DIMM.

Organized as 64M x 72, the SDRAM is packaged in a Fine Ball Grid Array (FBGA), mounted on a 244-pin DIMM FR4 substrate. This package is designed for a variety of high-bandwidth, high-performance memory system applications. It utilizes synchronous design, allowing precise cycle control with the use of a system clock. The module offers gold edge contacts, is dual rank and includes multiple internal device banks for concurrent operation.

The module features fast data transfer rates of PC2-6400, PC2-5300, PC2-4200 and PC2-3200, on-die termination and PLL. Features include programmable CAS# latency and posted CAS# additive latency, serial presence detect with EEPROM and differential data strobe for transmitting and receiving data. The module, part number W3HG264M72EER-AD7, is priced at $145 each in volumes of 1,000.

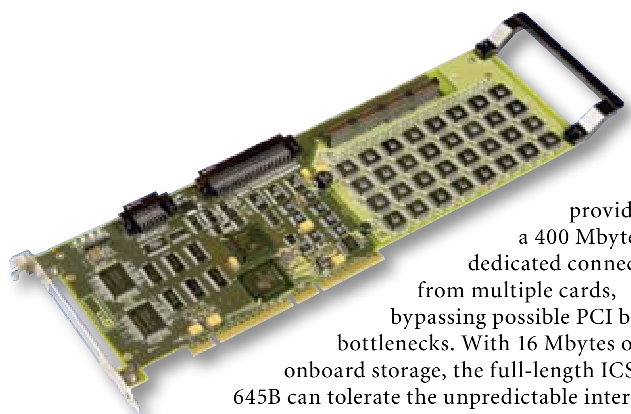


White Electronic Designs, Phoenix, AZ. (602) 437-1520. [www.wedc.com].

High-Speed A/D Data Acquisition Board Targets High-Frequency Apps

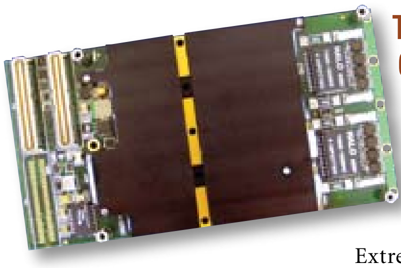
In high-frequency sonar, test and measurement and radar applications, the primary challenge of a high channel count, high-speed A/D converter card is moving data to the host processor or recorder. A data acquisition board from ICS, part of Radstone Embedded Computing, tackles this problem by providing two high-bandwidth data paths for communication with host systems.

The ICS-645B's 64-bit/66 MHz PCI interface provides sustained aggregate data rates in excess of 300 Mbytes/s, while the FPDP II port provides a 400 Mbyte/s dedicated connection from multiple cards, bypassing possible PCI bus bottlenecks. With 16 Mbytes of onboard storage, the full-length ICS-645B can tolerate the unpredictable interrupt latencies encountered in non-real-time operating systems. It provides 32 single-ended 16-bit A/D converter input channels, simultaneously sampled even in multi-card systems by high-speed oversampling Analog Devices AD9260 A/D converters at up to 20 megasamples/s.



Options include 8x, 4x, 2x and 1x oversampling modes. Windows and Linux device drivers and MatLab libraries are available. Pricing starts at $8,580.

Radstone Embedded Computing, Billerica, MA. (800) 368-2738. [www.radstone.com].



T1/E1/J1 PMC Is Conduction-Cooled

In the harshest environments, heat, cold, shock and vibration can destroy mission-critical military telecommunications hardware. A new conduction-cooled T1/E1/J1 PMC from Extreme Engineering provides telecommunications support for multiple protocols and interfaces in applications such as PBX-to-VoIP gateways, ISDN PRI, PCM voice, LAN/WAN data transport, frame relay, Signaling System 7 (SS7) and wireless basestations.

The conduction-cooled PowerQUICC II-based XPort2001 is the industry's first to support the Asterisk PBX. It supports fully channelized HDLC and transparent protocols over four software-configurable T1/E1/J1 interfaces, and includes CSU/DSU support. The card's Freescale MPC8270 Power QUICC II processor runs at up to 450 MHz. Up to 256 Mbytes of ECC DDR SDRAM and up to 64 Mbytes of soldered flash are provided, along with four T1/E1/J1 software-configured interfaces on the P14 rear I/O.

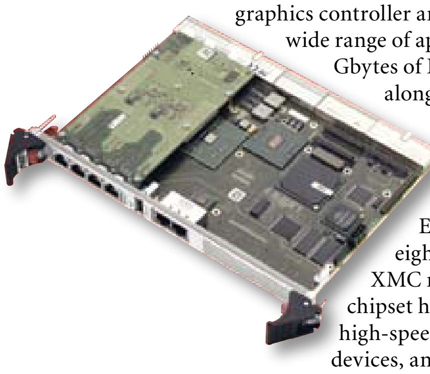
Operating temperature range is -40° to +85°C, and power consumption is under 4W. Options include 10/100 Mbit/s Ethernet on the P14 rear I/O, an RS-232 SMC port and SS7 support. Integrated PCI Asterisk software drivers are available for Linux. Linux and VxWorks BSPs are also available. OEM pricing is under $2,000, depending on memory configuration, processor clock speed and annual volumes.

Extreme Engineering Solutions, Madison, WI. (608) 833-1155. [www.xes-inc.com].

SBC Blade Server Targets Aviation and Defense Apps

Blade servers used in mission-critical communication systems call for high compute bandwidth and I/O throughput, as well as rugged design. A new 6U CompactPCI SBC from Men Micro has all three.

The 64-bit/66 MHz D6 system controller board features a Pentium M or Celeron M processor. An onboard FPGA implements the board's graphics controller and lets the board support a wide range of application-specific I/O. Up to 2 Gbytes of ECC DDR2 DRAM is included, along with non-volatile FRAM and SRAM application memory. Sixteen of the D6's 24 PCI Express lanes are devoted to the board's two Gigabit Ethernet interfaces. The other eight are used for one or two XMC modules. The 7520 Intel server chipset has two SATA interfaces for high-speed connections to mass storage devices, and an onboard PATA interface is available for a hard disk or CompactFlash storage. An Intelligent Platform Management Interface (IPMI) is included for monitoring and controlling critical onboard parameters.



Pricing for the version with a 2 GHz Pentium M and two XMC sites starts at $2,994 for single units.

Men Micro, Lago Vista, TX. (512) 267-8883. [www.menmicro.com].

COTS View

Software Modernization Is Key to Controlling Costs, Complexity

As electronics and computing hardware grow more complex, the costs and complexities of military software development get harder to control. A move to modern languages like Java help smooth the way.

Dave Wood, Director of Marketing
Aonix

The ongoing rapid evolution of hardware capabilities and capacities presents a double-edged sword for mission-critical applications. Hardware advancements boost functionality and performance, but also multiply complexities. And that means expanded software requirements, which in turn can add fragility and expense to the system development.

Doubling memory capacity or processor throughput may add only a few dollars to the cost of the hardware, but changing the software to take advantage of such increased capacity can add many millions of dollars of cost. If the technology used to build the software does not scale well, the applications will be error-prone and difficult to maintain.

These trends hold true not only in military applications, but across the spectrum of commercial applications as well. According to Anthony Scott, CTO of General Motors, more than one-third of the cost of GM's automobiles now involves software and electronic components, and the amount of software loaded into a typical automobile is skyrocketing. The amount of software in the average automobile has grown from 1,000,000 to over 32,000,000 lines of code in the past 15 years

In the face of this kind of growth in complexity, the continued use of aging methods and tools is a recipe for obsolescence and mission failure. For military systems, this problem is compounded by the fact that defense systems require the highest levels of reliability and longevity.

Modernization is essential not only to achieving the mission, but to doing so with an affordable cost and schedule. The challenge for the military is to determine what level of modern-

Figure 1

For the DD(X) destroyer program—now called DDG-1000—software developers have pushed the envelope of Java real-time garbage collection technology. Release 4 of the DD(X) software environment will switch completely to a real-time Java VM.

ization is necessary and the most efficient way to move software forward while leveraging legacy applications. Choice of language platform plays a central role in the success of any software modernization effort.

That language shift is already well underway in numerous very large and complex military applications that are now under active development using Java. Some that can be publicly identified include Future Combat Systems (FCS) and DDG-1000 (Figure 1) (formerly DD(X)). Java is relatively new for real-time and embedded systems, but its current expansion into mission-critical development is the result of several years of ongoing efforts to develop Java technologies to meet the specialized needs of mission-critical systems. In fact, the DDG-1000 software developers have pushed the envelope of Java real-time garbage collection technology. Release 4 of the DD(X) software environment will reportedly switch completely to a real-time Java VM.

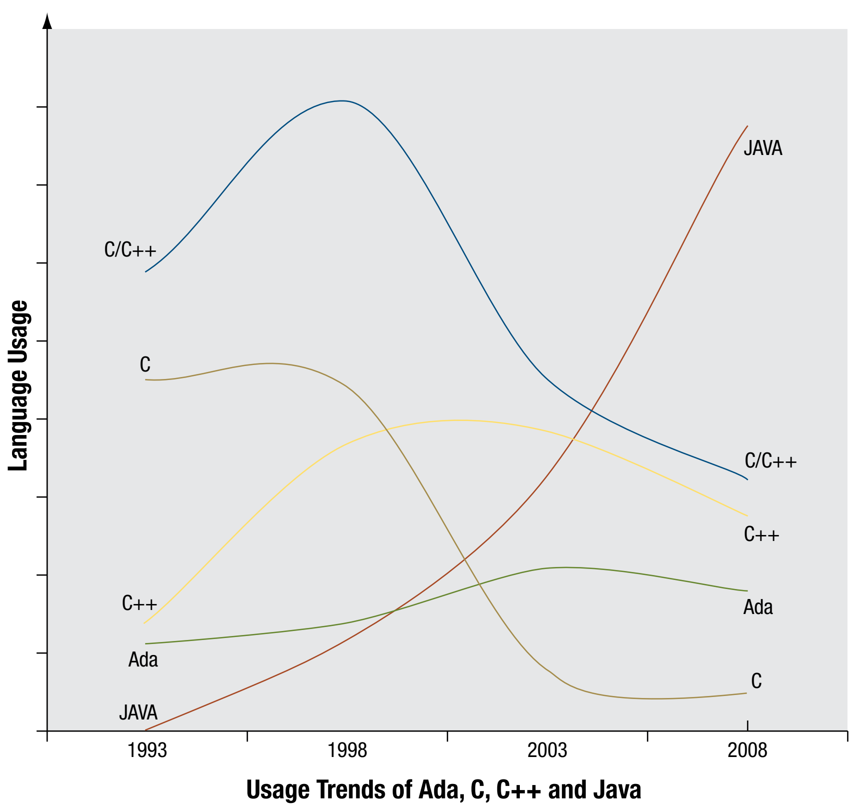


Figure 2

Over the past decade, Java has taken over as the language and platform of choice on the desktop, Web and mobile applications, widely displacing C and C++ in those application areas. The dominance of Java has resulted in substantial improvements in quality and productivity due to the wide availability of Java-trained engineers and thousands of standardized and reusable off-the-shelf components.

Paths to Modernization

Software modernization holds that software systems can benefit from the migration of legacy approaches to more modern and current approaches. If conducted successfully, modernization ensures that software engineering can keep pace with the ongoing evolution of hardware capabilities.

Modernization means different things in different situations. In some circumstances, it is desirable to retain a successful and well-designed legacy application, while enhancing its functionality by incorporating modern components. In other cases, it's best to transform an existing system written in an older language, running on older hardware, to a more COTS-friendly language and platform. Transformation techniques have been studied and described by Boeing, Semantic Designs, ArtiSoft and others. Such techniques promise preservation of quality design components and savings on re-engineering costs, although they do not specify by which criteria we should select methods, tools, platforms and languages.

In order to avoid repeating past mistakes, it is desirable to modernize not just a specific application, but the entire thinking behind the software development. By doing this, the development of new applications or new components of legacy applications is most productive, reducing error incidence and heightening scalability and reuse. Whether modernizing individual components, a complete application, or the software development process, language selection plays a central role in modernization success.

Productivity and Reliability

Today, most embedded and real-time systems still are built using C and C++ languages. Mission-critical applications include significant legacy code built with languages such as Jovial and Ada. Ironically, the COTS movement with its focus on implementing off-the-shelf technology, has helped drive mission-critical development increasingly from Ada to C++. Given the lower error rates and superior software engineering aspects offered by Ada, the trend of the past decade to use C++ for new design wins can be viewed as a move in the wrong direction. On the other hand, Ada is seen by many as lacking the COTS desirable traits of broad commercial acceptance and widespread use in academia and emerging engineering talent pools.

A case can be made to move from Ada based on achieving COTS ideals, but the abandonment of the engineering principles

What Makes Java Suited for Real-Time Apps?

The NIST Requirements Group considers these Java traits to provide a basis for the real-time requirements and motivation for Java's use by the real-time community:

- Java's higher level of abstraction increases programmer productivity.
- Java is easier to master than C++.
- Java is secure, keeping software components (including the JVM itself) protected from one another.
- Java dynamically loads new classes.
- Java is highly dynamic, supporting object and thread creation at runtime.
- Java supports component integration and reuse.
- The Java development process is conservative using concepts and techniques that have been scrutinized by the community.
- Java language and platforms offer application portability.
- Java technologies support distributed applications.
- Java provides well-defined execution semantics.

embodied in Ada should not be done lightly. Despite positive features such as widespread commercial acceptance, the selection of C++ as the language of choice is problematic from the perspective of modernization. The critical principles of modernization demanded by the rapidly increasing complexity of mission-critical software are productivity and reliability. C++ has not shown itself to scale well with regard to the productive development of reliable software.

In looking for a suitable alternative, Java emerges as the natural choice since it provides the commercial success and vast technology ecosystem that has eluded Ada, while also achieving superior scalability, portability, memory security and simplicity issues compared to C++, while following a familiar C-based syntax.

The problems inherent in C and C++ are well documented. Twenty years ago, when most real-time systems were developed in assembly language on bare hardware, C offered an advancement, representing a first-level abstraction away from the hardware level. Over time, C has evolved into C++, adding object orientation and many other useful features, although many people who use C++ compilers continue to confine themselves to the C subset of the language.

Unfortunately, the benefits offered by the substantially more complex C++ language do not include corrections for serious error-prone attributes of C, such as type insecurity and easily abused memory management. These attributes of C/C++ can be overcome by top quality technique, which should always be a goal. However, reliance on top quality technique is an approach that simply does not scale up well without prohibitive cost. It is a better use of costly engineering talent to automate reliability factors as much as possible so that engineers can focus on functionality and design efficiency.

With rapidly growing software complexity, the importance of productivity cannot be overstated. To continue development focused on the C++ language will result in an exponential rise in software costs for the military.

Why Pick Java?

As an alternative, Java programming is as much as two times more productive than C++, six times less burdensome

Ada is seen by many as lacking the COTS desirable traits of broad commercial acceptance and widespread use in academia and emerging engineering talent pools. A case can be made to move from Ada based on achieving COTS ideals, but the abandonment of the engineering principles embodied in Ada should not be done lightly.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Application Domain	Number Projects	Size Range (KESLOC)	Avg. Productivity (ESLOC/SM)	Range (ESLOC/SM)	Example Application
Command & Control	45	35 to 4,500	225	95 to 350	Command centers
Military - Airborne	40	20 to 1,350	105	65 to 250	Embedded sensors
Military - Ground	52	25 to 2,125	195	80 to 300	Combat center
Military - Missile	15	22 to 125	85	52 to 175	GNC system
Military - Space	18	15 to 465	90	45 to 175	Attitude control system
Trainers/Simulations	25	200 to 900	225	143 to 780	Virtual reality simulator

ESLOC = equivalent source lines of code; SM = staff-month

Table 1

Historically, mission-critical applications are produced at a rate of only 45-780 source lines of code per staff-month. Source: DoD Software Tech News.

in terms of error creation, detection and correction, and much more portable across hardware architectures. Based on industry-wide productivity averages (Table 1), even modest productivity enhancements can shave hundreds of thousands of dollars off development costs and improve time-to-deployment by many months. To those who have not considered the human cost of software development, the impact of productivity improvements on real-world cost savings can be surprising. Based on observed Java productivity figures, lifetime savings for a moderate-sized mission-critical application can amount to several million dollars, while providing much higher reliability, superior scalability attributes and faster deployment.

Over the past decade, Java has been the language and platform of choice on the desktop, Web and mobile applications, widely displacing C and C++ in those application areas. In Figure 2, we see how the emergence of Java has resulted in substantial improvements in quality and productivity due to the wide availability of Java-trained engineers and thousands of standardized and reusable off-the-shelf components.

Beginning in 1997, the National Institute of Standards and Technology coordinated the activities of an expert group in defining the requirements for the use of Java in real-time and embedded development. The NIST group, comprising over 50 major technology companies including Sun, IBM, Microsoft, Aonix, Wind River, Motorola and QNX, drew the conclusion that Java has the traits required to improve productivity and quality for real-time systems. For a list of those traits, see the sidebar "What Makes Java Suited for Real-Time Apps?" in this article.

Following the conclusion of the NIST efforts, several years of specification, research and development efforts were undertaken by commercial companies to develop the first solutions for real-time Java developers. The primary concerns in creating an implementation were the needs of the real-time and embedded community, including:

- Small memory footprint
- Fast response times
- High execution throughput
- Access to low-level devices
- Management of increasingly complex applications
- Reduction of error incidence
- Facilitation of error detection and removal

These efforts have resulted in the emergence of a variety of technologies. For example, the introduction of predictable, real-time garbage collection within Java Standard Edition semantics has been very capable and successful in applying the modern advantages of Java to complex mission-critical applications.

Ongoing efforts through the Open Group are driving emerging standards for deeply embedded, resource-constrained and safety-critical application development through the Java Community Process based on specialized profiles of the real-time specification for Java (RTSJ). The first such technologies are now coming to market, providing a bridge to modernization for mission-critical applications requiring footprint and performance comparable to C and C++ applications, while retaining the scalability and reliability of Java. New systems can be developed in Java with integration to legacy components for expedience. Over time, legacy components, even those "close to the silicon" can be ported directly to Java code, without loss of capability or performance.

By taking advantage of such technologies, mission-critical program offices now have the ability to fight encroaching obsolescence and to modernize both legacy and new applications by tapping into the vast resources of Java libraries and components, while taking advantage of the growing stream of Java-aware developers emerging from universities. ▮▮

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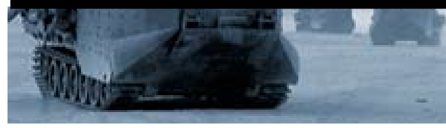
Coming Next Month

Take that last trip to the beach, grill that last burger. Just a handful of summer weekends left. We're already back on the job getting our August issue ready. Take a look at what we're wrapping up for our August issue:

- *Military-Specific I/O.* Tried and true I/O schemes, such as MIL-STD-1553 and ARINC 429, remain popular for pure command control applications. But they're bandwidth-limited by today's standards. A slew of multipurpose communications protocols provide options to suit emerging needs. Articles in this section compare today's crop of I/O schemes relevant to military users.
- *Cooling Technologies.* The trend toward processors and other key components ramping up in wattage is unavoidable. And more power means more challenges dissipating heat. Exotic techniques such as spray-cooling and liquid-cooling are all on the table as possible ways to attack the cooling challenge. Articles in this section touch on all those present-day and future cooling solutions.
- *Bus Analyzers.* Bus- and protocol-specific analyzers are critical tools for any modular embedded computer designers. Now they are more important than ever as military system designers make the shift from parallel bus-based systems to architectures based on switched fabrics like PCI Express and others. VME and cPCI standards groups have already incorporated PCIe and other fabrics into their next-gen specs. This Tech Focus section updates readers on analyzer trends and explores the problems they're solving for defense applications.
- *3U CompactPCI.* The CompactPCI embedded form-factor—now well into its second decade of existence—has achieved the maturity and broad product range that military system designers so crave. The 3U flavor of cPCI is particularly attractive to space/weight-constrained applications like avionics. This Tech Focus section updates readers on 3U cPCI trends, and provides a product album of representative conduction-cooled 3U cPCI boards.



COTS

Editorial

Jeff Child, Editor-in-Chief

UAVs Getting Out of Joint

There's no doubt that Unmanned Aerial Vehicles (UAVs) boast the most dramatic success story in military electronics technology over the past decade. UAVs—of many varieties—have performed extremely well during recent conflicts in the Middle East. Aside from their most important benefit—performing missions that would otherwise put servicemen in harm's way—they've played a vital role in identifying time-critical targets that can then be struck by manned and unmanned aerial platforms. Moreover, UAVs have been an extremely cost-effective investment. Consider that UAVs comprise only around 10 percent of the total DoD annual budget, and they fly over 80 percent of the U.S. Military's aviation hours per year.

All that said, UAV development efforts are in danger of falling short of their full potential benefits—in operational capabilities and cost-savings—because of a lack of standards and insufficient focus on interoperability. It's not like the DoD isn't aware of this unfortunate trend. In its 2005 to 2030 Unmanned Aircraft Systems Roadmap, the Secretary of Defense's UAS Planning Task Force cited that many UAVs have been developed with limited attention to Joint interoperability requirements.

Meanwhile, at the end of last year, the Government Accounting Office (GAO) released a report that criticized the Joint Services interoperability of UAVs. The report acknowledged that the DoD's guidance called for interoperability, however, in practice, detailed standards for such interoperability have not been developed. Instead, the Service Branches have developed differing systems that rely on technical patches to permit interconnection at much slower data rates. Another issue is the interchangeability of sensors and platforms.

Programs have suffered from a lack of standardized sensor products, lack of standardized meta-data for both sensors and platform information, and lack of a common tasking system that crosses the traditional command boundaries. Again, lack of a payload commonality standard causes availability issues and delay if compatible unmanned aircraft and payloads are not available. Given that U.S. forces develop, procure and operate UAVs as service-specific programs, it's not unexpected that they aren't that attentive to Joint needs.

An example of where a closer link between branches seems called for is the Fire Scout, a Vertical Takeoff and Landing Tactical Unmanned Aerial Vehicle (VTUAV) being developed for the Army and the Navy. Although Fire Scout isn't technically a Joint Army/Navy program, the two branches are cooperating closely on it. The Army selected Fire Scout as its Class IV UAV for its Future Combat Systems program.

For the Army Fire Scout, Northrop Grumman provides just the air vehicle for Boeing and SAIC—the Lead System Integrators for FCS—while Boeing does the avionics, including a different control system than the Navy version and a different datalink. While the Navy Fire Scouts are scheduled to go into services in FY 2008, the Army Fire Scouts, for now, will have to go into storage until the Future Combat Systems program can make use of them. Hindsight is 20-20 of course, but it's easy to imagine a lot more commonality of electronic subsystems between the Army and Navy Fire Scouts.

Another standards-related problem in UAVs is the lack of electromagnetic spectrum. UAVs demand a lot of bandwidth resources for control uplink and imagery downlink. Lack of standards makes it necessary for redundant subsystems to make use of bandwidth resources. While the latest UAV systems are adapting common datalink systems, many deployed systems will be difficult to change to avoid bandwidth congestion.

Interoperability problems will magnify as the number UAVs and UAV types ramp up. Forecasts of the overall worldwide market (not just for defense) show a lucrative future for makers of UAVs. Market research firm Visiongain released a report in May that predicted UAVs would top $15 billion in the next decade up from only around $2.4 billion in 2000. U.S. firms hold more that half the market now, but could gain as much as 10 percent more of it over the next decade.

As all branches of the U.S. Military ramp up their number of UAVs, the interoperability problem will expand and become harder to reverse. Programs that can boast cost-effectiveness and stellar operational success—as most UAV programs can—tend to sail along without waiting for standards. Certainly a number of broad standards will gain traction in future UAV programs—for instance, a migration to JTRS/SCA-compliant capability when that becomes available—but I don't hold out a lot of hope for much top-down standardization among modular subsystems useable across a variety of UAVs and classes of UAVs.

What may be required is a bottom-up push from the embedded computing industry. This industry should create platform standards aimed at various UAV payload, communications and control functions. Those could enable an enormous cost-savings in overall UAV development along with an increased opportunity for our industry to sell board-level embedded solutions into the fast growing UAV market. ❚❚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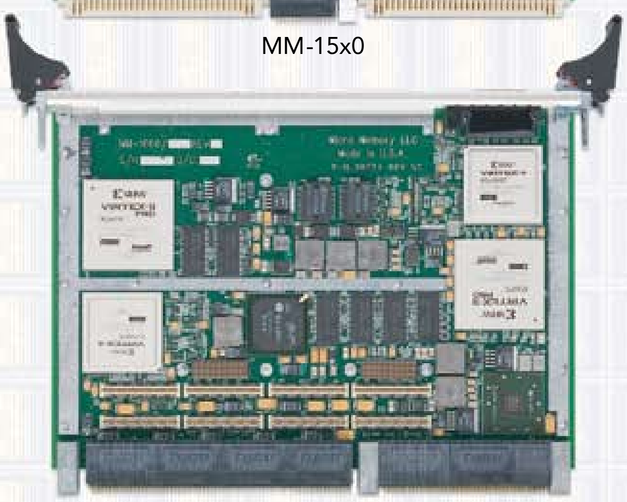

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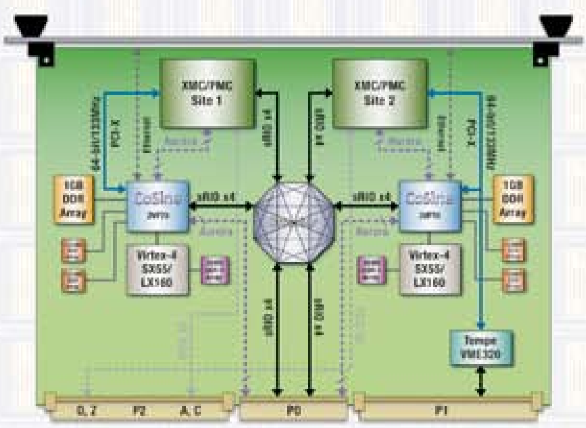

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